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Low Power Three-Input XOR/XNOR with Systematic Cell Design Methodology

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Abstract - The rapid growths of portable electronic devices are increased and they are designing with low power and high speed is critical. To design a three input XOR and XNOR gates using the systematic cell design methodology can be achieved by implementing transmission gate. By this type of designing the low power and high speed can achieved. This architecture is used to maintain summation results for after completing addition process. To reduce the overall leakage power level and size of the circuit, this simulation is carried out using TSMC 90nm in Tanner EDA Tool.

***Keywords* - XOR/XNOR Circuits, SCDM, Hybrid CMOS, Transmission Gate.**

1. Introduction

The rapid growth of portable electronic devices is a critical challenge to design low-power, high-speed circuits that occupy small chip areas. Such studies mostly rely on creative design thoughts but do not follow a systematic approach. As an importance, most of them suffer from some different drawback.

1. They are implemented with logic styles that have an incomplete voltage swing in some internal nodes, which leads to the static power dissipation.
2. Most of them undergo from severe output signal degradation and cannot sustain low-voltage operation.
3. They predominantly havea dynamic power consumption fornon-balanced propagation delay inside and outside circuits, which results in glitches at the outputs.

A well-organized design methodology can be regarded as a strong clarification for the challenge. It is not try-and-error-driven, which means that it systematically and intentionally aims to a design goals. It also picks circuit components wisely and does not postpone the determination of the circuit characteristics after simulation. Cell design methodology (CDM) has been presented to design some narrow functions, such as two-input XOR/XNOR and carry–inverse carry in the hybrid-CMOS style. The predominant results persuade us to develop CDM through two stages:

1. Generating more complex functions and
2. Rectifying some remaining flaws.

The exclusive-OR (XOR) and exclusive-NOR (XNOR) gate is the critical parts of several digital systems and it is highly used for very large scale integration (VLSI) system. The XOR/XNOR circuits used in parity checkers, comparators, crypto processors, arithmetic and logic circuits , test pattern generators. The SCDM methodology for design a XOR/XNORs gate and design is implemented. The first time Systematic Cell Design Methodology (SCDM) designing a three-input XOR/XNORs. Its systematically generates elementary basic cell (EBC) by using the binary decision diagram (BDD), and wisely chooses circuit components based on a specific target. Therefore, after the systematic generation, the SCDM considers circuit optimization based on our objective in three steps:

1. Wise selection of the basic cell;
2. Wise selection of the amend mechanisms;
3. Transistor sizing.

The motivation to use this methodology is the presence of some unique features and the capability to produce some effective circuits that enjoy all these benefits.

1. The methodology has high flexibility in goal and systematically considers it in the three design steps. This can lead to effective circuits in terms of performance, power, Power Delay Product (PDP),Energy Delay Product (EDP), area, or a combination of them.

2. Systematic Cell Design Methodology (SCDM) develops the aids of different logic styles as the hybrid-style.
3. The least number of transistors in critical path increases the chances of the circuit to have better characteristics.
4. The dynamic consumption optimization comes from the fact of well-balanced propagation delay.
5. Symmetrical structure, high modularity, and regular arrangement of designs give increase to sharing more wells of connected transistors and in turn reducing the occupied area.
6. The degradation in all output voltage swing can thus be finally removed, which makes the design sustainable in low V_{dd} operations and low static power dissipation.
7. Internal logic structure of designs has the potential to be energy efficient and due to the combined reduction of power consumption and propagation delay.

2. Design and Implementation

2.1 SCDM for Three-Input XOR/XNOR Circuits

The methodology for three-input XOR/XNORs are presented according to the flowchart shown in Fig. 1(a).In the first stage, a three-input XOR/XNOR as one of the most complex and all-purpose three-input a basic gate in arithmetic circuits has been chosen. If the efficiency of the circuits is confirmed in such aneconomic environment, it canbe show that the strength of the methodology. In the second stage, Cell Design Methodology is matured as systematic Cell Design Methodology (SCDM) in designing the three-input XOR/XNORs for the first time. It systematically generates elementary basic cell using binary decision diagram, and wisely chooses circuit components based on a specific target. This takes place when the mentioned features are not considered in the Cell Design Methodology.

After the systematic generation, the SCDM considers circuit optimization based on our target in three steps: 1) the wise selection of the basic cell; 2) the wise selection of the amend mechanisms; and 3) the transistor sizing. It should be noted that BDD can be utilized for EBC generation of other three-input functions. We consider the power-delay product as the design target. It stands as a fair performance metric, precisely involving portable electronic system targets.

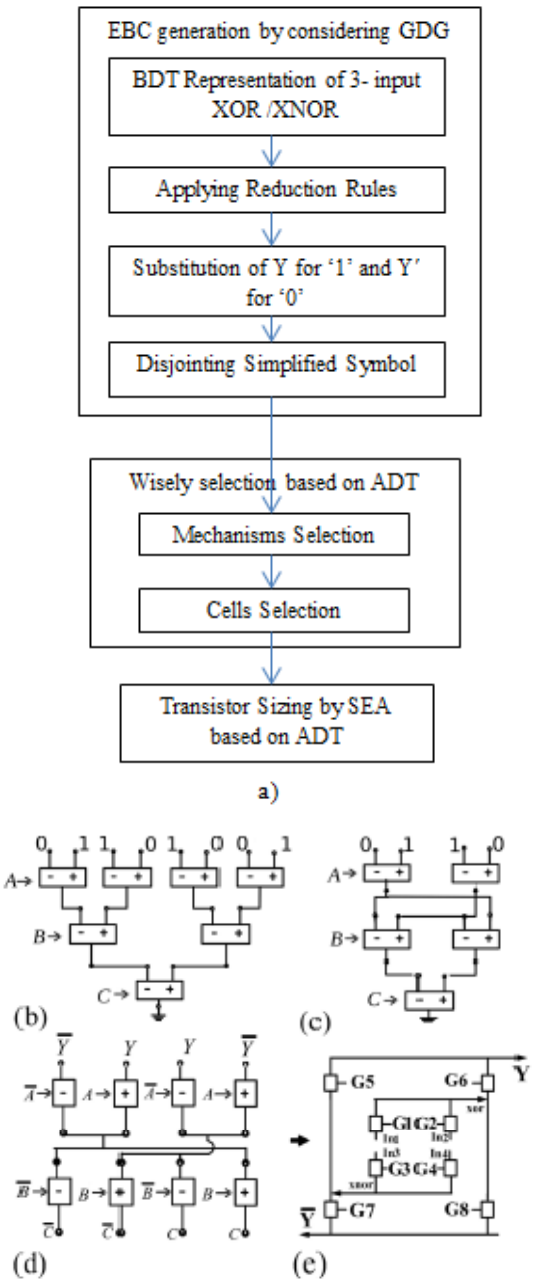

Fig.1. (a) SCDM process for designing efficient three-input XOR/XNORs. (b) BDT representation of three-input XOR/XNOR function. (c) Applying reduction rules. (d) Substitution and disjointing. (e) EBC.

2.2 Elementary Basic Cell Systematic Generation

In order to generate the Elementary Basic Cell (EBC) of three-input XOR/XNOR circuits, four steps are taken. Initially, three-input XOR and its complement are represented by one binary decision tree in order to share common sub circuits. The BDT is achieved by some cascaded 2 ×1 MUX blocks, which are denoted by the basic symbol controlled with input variables at each correspondent level. This construction simply

implements the min-terms of the three-input XOR/XNOR function. This step is followed by applying reduction rules to simplify the BDT representation. This includes elimination, merging, and coupling rules. The major task of the coupling rule, in simple terms, is to obtain all the possible equivalent trees by interchanging the order of the controls.

The result of applying the reduction rules of the tree. Afterward, the inputs into the first level are 0's and 1's of the function's truth table, the 0 and 1 can be replaced by the Yand Y′, correspondingly. Finally, the simplified symbol can be divided into two distinct symbols: 1) the plus sign with the x input control and 2) the minus sign with the *x*′input control. The result of applying steps 3 and 4. The EBC, which is extracted from the above procedure, has been presented. This cell has eight elements, deciding two outputs. We refer that the pins of the central section (IN1–IN4 and G1–G4) as A or C, or their complements. We also adopt that pins of the external section G5–G8 can also be B or its complement.

2.3 Wisely Selection of Mechanisms and Cells Based on Design Target

The replacing elements with pass transistors or transmission gates and the control inputs with input signals in combination with optimization and correction mechanisms, a huge circuit library is achieved as each circuit can be appropriate for specific applications. The selection is meditated to determine dominant mechanisms and cells, in terms of PDP, power, and delay when the optimization goal is PDP. The results are used to produce circuits for high-performance portable electronic applications. This Mechanisms include optimization mechanisms to resolve non-full swing inverter and feedback , correction mechanisms to resolve high impedance pull up-down network and feedback , or the combinations of them bootstrap-pull up-down, feedback pull up-down, bootstrap-feedback , inverter-feedback , and inverter-pull up-down.

Taken all the above points collectively, under the assumptions about the technology and the domain of circuits, the specific mechanism, I, does not present proper performance in terms of power and delay. This is while it was introduced as the only solution for nonfull swing outputs in many papers. Due to the high power consumption, I in combinational mechanism, such as IF and IP, operate worse than both BF and BP.The high impedance problem is also improved resolved by P as we can observe IP to IF and BP to BF perform superior. Resulting, using transmission gate in EBC and TG enjoys the least power, delay, and PDP as a complete part that does not need any mechanisms.At the end, the separate mechanism, F, with suitable transistor sizing is accomplished of playing a key role besides the dominant combinational mechanisms, BP and FP, for the wisely design when PDP is target. Furthermore, the analytical expressions of optimum frequency and the supply voltage under minimum energy condition have been verified through simulation in 90-nm technology.

2.4 Transmission Gates

Complementary Metal Oxide Semiconductor (CMOS) is a technology for integrated circuits. The CMOS circuits use a combination of p-type and n-type Metal Oxide Semiconductor Field Effect Transistor (MOSFETs) to implement logic gates and other digital circuits. The transmission gate is made up of two field effect transistors thus the transistors are n-channel MOSFET and p-channel MOSFET are connected with parallel with each other. In that the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other via a NOT gate (inverter), to form the control terminal. Atransmission gate must block flow in either direction thus the substrate terminals are connected to the supply voltage. The substrate terminal of the p-channel MOSFET is connected to the positive supplyvoltage and the substrate terminal of the n-channel MOSFET are connected to negative supply voltage.

2.5 Advantages of Transmission Gate

1. Logic circuits can be constructed with the relief of transmission gates instead of traditional CMOS pull-up and pull-down networks.
2. The circuits can frequently be made more compact, which can be an important consideration in silicon implementations.
3. In a security application, they can selectively block critical signals or data from being transmitted without suitable hardware-controlled authorization.

3. Introduction of the Structure of Three-Input XOR/XNOR Circuits with the Average PDP in Femtojoule

TABLE 1: The average PDP in FEMTOJOULE

Circuits	centeral part				external part				avg PDP
	BC	mechanisms F	B	P	BC	mechanisms F	B	P	
XO1	TG				C1	Fnp	-	-	1.27
XO2	C2	Fnp	-	-	C2	Fnp	-	-	0.70
XO3	TG				C2	Fp	-	-	0.62
XO4	TG				TG				0.42
XO5	TG				C1	Fnp	-	✓	0.71
XO6	C2	Fnp	-	-	C2	Fnp	-	✓	0.57
XO7	TG				C2	Fp	-	✓	0.47
XO8	TG				C1	-	p&n	✓	0.86
XO9	C2	Fnp	-	-	C2	-	p	✓	0.65
XO10	TG				C2	-	n	✓	0.50

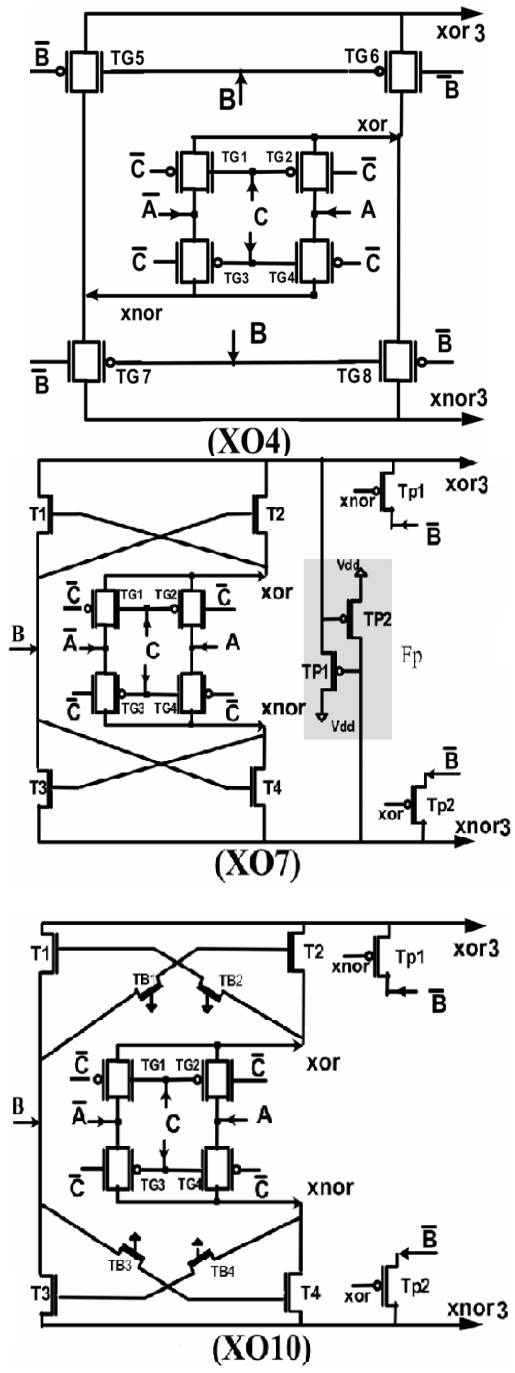

Fig.2 Three-input XOR/XNOR circuits, XO4, XO7, and XO10.

The three input XOR/XNOR gates are realized using the transmission gate logic. Thus the transmission gate is a design of parallel connection of PMOS and NMOS. By using this gate design the three input XOR/XNOR gates are realized and thus the logical operations of gate are achieved in the result. The three input XOR/XNOR circuits XO4, X07, XO10 is shown in the Fig.2.

To control the capacity of this brief, only the simulation results of the conventional and three of the best proposed circuits in terms of average PDP according to Table 1, XO4, XO7, and XO10, are tabulated in Table. The ascending order of delay, which is the maximum delay between all the possible transitions, as well as PDP it is apparent that among the circuits XO4 and XO7 have the reduced delays. The circuit of XO7 has slightly less delay than the XO4 at lower supply voltages. However, the trend will reverse at higher supply voltages. Hernandez1 has the second position. The circuits XO10, Transmission Feedback (TF), and 16 T_NEW_FS follow the Hernandez1. In the common circumstances, the circuits utilizing FP, such as XO7 is superior to the circuits utilizing BP like XO10, which is compatible with the delay trend of mechanisms. The circuits with *C*2 like XO10 and XO7 also perform better than the circuits with *C*1. Since bootstrap technique saves the internal node voltages, the average power dissipation underneath different supply voltages shows that PB has less power dissipation in common situation. XO10 employing BP outperforms XO7 employing FP with regard to average power.

According to the PDP trend, the ability of TG to provide full-swing leads to the best circuit with optimum performance and drivability as among the circuits, XO4 has the lowest PDP. After that, circuits XO7 and XO10 have the second and third position, respectively. PDP of XO7 is less than that of XO10 for lower voltages but the movement reverses for higher voltages. Hence, from energy point of view, XO7 is anenhanced choice. The circuits, such as XO7 using FP outperform the circuits using feedback. The circuits with *C*2 like XO7 and XO10 offer less PDP than the circuits with *C*1.

4. Simulation Result

4.1 Schematic Diagram ofXO10 Circuit

The Fig.3 shows that a schematic of XO10 was simulated in S-Edit of Tanner EDA tool. This circuit consists of two parts one is central part and another one is external part. Central part consists of four transmission gates which are connected in such a way that it gives the XOR/XNOR output of two inputs. And the external circuit consists of four transmission gates. This part takes the output of central part output as one input and the other one is direct input. The total output of the circuit can collect at external part which is three input XOR/XNOR output. As XO10 was designed using transmission gate technology for internal part and Pull-up, pull-down network technology for external part. It shows some voltage degradation in their output.

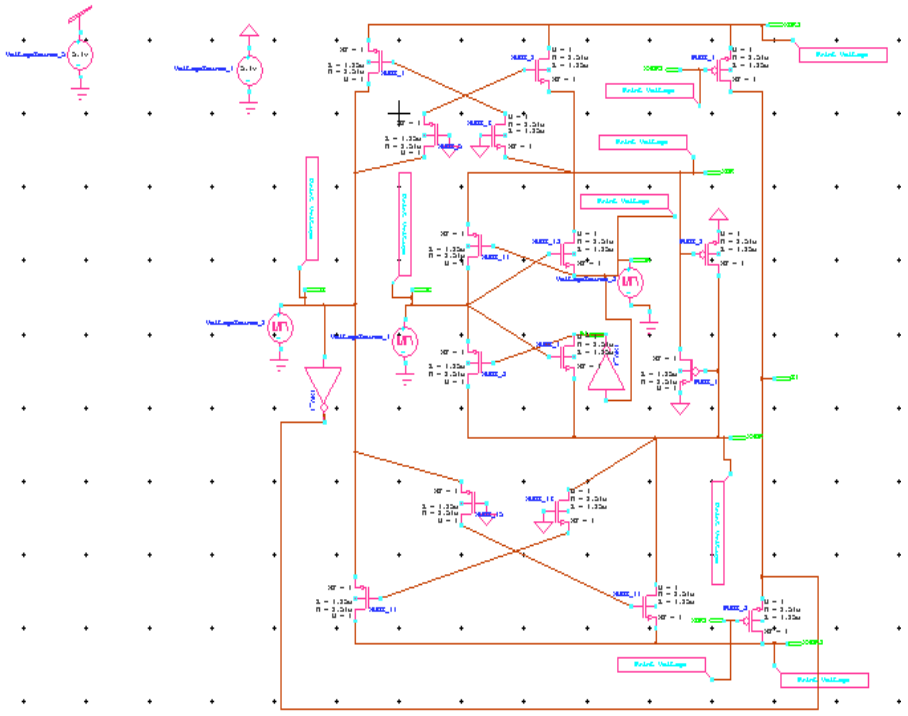

Fig.3Schematic diagram of the XO10 Circuit

4.2 Simulation Result of XO10

The below Fig.4(a) shows the XO10 simulation waveform with V(A), V(B), V(C) as inputs generates V(XOR) and V(XNOR) as outputs.

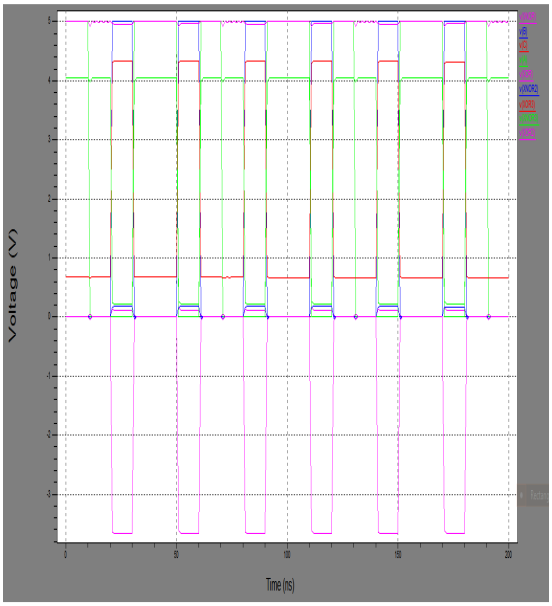

Fig.4 (a) Schematic Waveforms of XO10 Circuit

The below Fig.4 (b) shows the XO10 simulation waveform with V(A), V(B), V(C) as inputs generates V(XOR) and V(XNOR) as outputs.

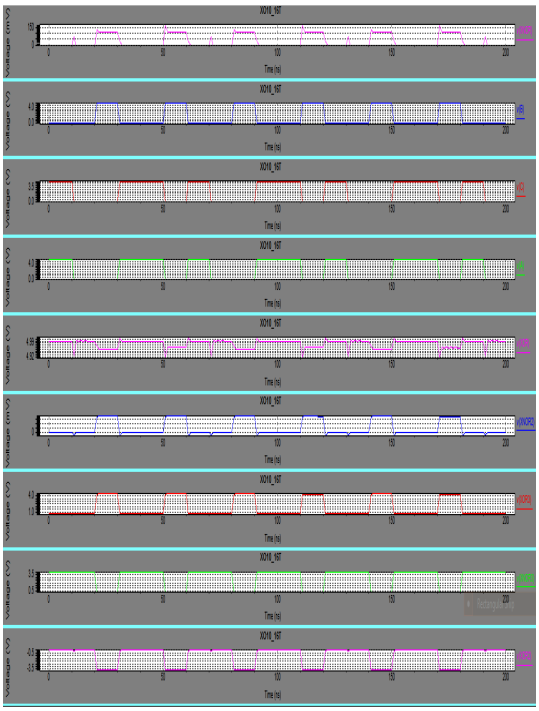

Fig.4(b) Schematic Waveforms of XO10 Circuit

5. Conclusion

To design a three input XOR/XNOR gate and the analytical expression of optimum frequency and supply voltage under minimum energy condition has been verified through simulation in 90-nm technology. The performance of the proposed circuits can operate at low-voltages, and have good output levels. According to the simulation results, the proposed circuit offers a better result and more competitive than other design. It offers the lowest power dissipation at a low supply voltage. It has a good driving capability with good output signal in all input combinations and well performance especially in low supply voltage compared to the previous designs. Thus, the proposed circuit is suitable for low-voltage and low-power application.In future work 8-bit adder architecture based on the design of three-input XOR/XNOR gate will be designed. The power consumption and delay performance are calculated and compared with the existing system.

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