IJCAT - International Journal of Computing and Technology, Volume 3, Issue 11, November 2016
ISSN: 2348 - 6090
www.IJCAT.org

Designing of High-Performance Carry Select Adder Using CMOS Technology

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Abstract - This paper presents a novel designing approach for high performance carry select adder(CSLA). As the demand for the portable equipment's like mobile phones and laptops increases in our day to day life. So, greater attention has to been focused in designing of processors that has less power consumption, low cost and have a better performance. Adders are the main building block of processors. The performance of the adder greatly influence the performance of the processors. To perform fast addition operation at a lower cost, carry select adder is most suitable among other adders. The carry select adder (CSLA) consists of full adders (FAs) and multiplexers. The proposed structure is assessed by the power consumption of the full adder using a 32-nm static CMOS technology for a wide range of supply voltages. The simulation results are obtained using Tanner EDA which reveals that full adder has low power consumption.

Keywords **– CSLA, FAs, & CMOS Technology.**

1. Introduction

Adders are the main building block in arithmetic and logic units (ALUs) and hence increasing their speed and reducing their power/energy consumption strongly influence the speed and power consumption of processors. There are many works on optimizing the speed and power of adders. Obviously, it is highly desirable to obtain higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors.

One of the efficient techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage. Moreover, the main leakage component in OFF devices, is the subthreshold current, which has an exponential dependence on the supply voltage level through the drain-induced barrier lowering effect. Based on the amount of the supply voltage reduction, the operation of ON devices may occupy in the super threshold, near-threshold, or subthreshold regions. Working in the super threshold region provide lower delay and higher switching and leakage powers compared with the near/subthreshold regions. the logic gate delay and leakage power exhibit exponential dependences on the supply and threshold voltages in the subthreshold region. In addition, these voltages are (potentially) subject to process and environmental variations in the nanoscale technologies. These variations increase the uncertainties in aforesaid performance parameters. For the circuits operating in the subthreshold region, the small subthreshold current causes a large delay.

Currently, the near-threshold region has been considered as a region that provides a more desirable tradeoff point between delay and power dissipation compared with that of the subthreshold one, because it results in lower delay compared with the subthreshold region and significantly lowers switching and leakage powers compared with the super threshold region. Moreover, near-threshold operation, which uses supply voltage levels near the threshold voltage of transistors, which considerably less from the process and environmental variations by comparing with the subthreshold region. The power (and performance) depending on the supply voltage has been the motivation for designing the circuits with dynamic voltage and frequency scaling. In these circuits, the energy consumption can be reduced by, changing the voltage (and frequency) of the circuit based on the workload requirement. For these systems, the circuit must be able to operate under a wide range of supply voltage levels. To obtain higher speeds at lower supply voltages for the computational blocks, with the adder as one the main components, might be crucial in the design of high-speed, yet energy efficient, processors. One of the biggest challenges related to low-power design is mitigating and controlling the leakage power of a circuit.

2. CSLA

The carry-select adder mostly consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers through a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the hypothesis of the carry being zero and the other with a hypothesis of one. Later the two results are calculated, the correct sum, as well as the correct carry out, is then selected with the multiplexer when the correct carry in is known. The basic building block of a carry-select adder[2], where the block size is 4 is shown in the Fig.1. The block size should have a delay when variable inputs are given to the circuit. In addition, inputs A and B to the carry out, equal to that of the multiplexer chain which leading into it, so that the carry out is calculated just in time. The delay is obtained from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits that being added, since that will yield an equal number of MUX delays.

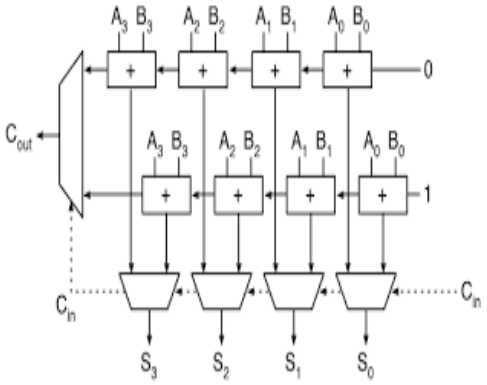

Fig 1. Block diagram of CSLA

If two 4-bit ripple carry adders are multiplexed together, where the resulting carryout and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption through the actual carry-in yields the correct result. Adding two n bit numbers with carry select adder is done with two adders. In order to obtain the calculation twice one time with the assumption of carry as 0 and other with assumption of carry 1. That is carry select adder consists of two ripple carry adder for which one is assumed with a carry 0 and other block with a carry 1. After two results are calculated the correct sum, as well as the correct carry out is then selected with the multiplexer once the correct carry in is known.

Carry select adder architecture consists of independent generation of sum and carry. That is carry in equal to zero and carry in equal to one are executed parallelly. Depending upon the carry in, the external multiplexers select the carry to be propagated to the next stage. Hence the delay is reduced. One of the biggest challenges related to low-power design is mitigating and controlling the leakage power of a circuit. Once considered a minor nuisance a decade ago has now become one of the top design priorities in modern microprocessors.

2.1 CMOS Technology

One of the most prevalent MOSFET technologies available today is the Complementary MOS or CMOS technology. CMOS technology is the leading semiconductor technology for microprocessors, logic memories and application specific integrated circuits (ASICs). The main benefit of CMOS over NMOS and BIPOLAR technology is the much lesser power dissipation. Unlike NMOS or BIPOLAR circuits, a CMOS circuit has virtually no static power dissipation. Power is mainly dissipated in case the circuit actually switches. This allows to integrate many more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much improved performance. In CMOS technology, both N-type and P-type transistors are used to realize the logic functions. The same signal which has to be turns *on* a transistor of one type is used to turn *off* a transistor of the other type. This allows the design of logic devices using the simple switches, without the need for a pull-up resistor.

In CMOS logic gates a group of n-type MOSFETs is arranged in a pull-down network between the output and the lower voltage power supply rail (Vss or quite often ground).CMOS logic gates have a set of p-type MOSFETs that form a pull-up network between the output and the higher-voltage rail (often named Vdd) but the NMOS logic gates have load resistor. Thus, if the gates of both p-type and n-type transistors are connected to the same input, the p-type MOSFET will be on when the n-type MOSFET is off, and vice-versa.

An important feature of a CMOS circuit is the duality that exists between the PMOS transistors and NMOS transistors. A CMOS circuit allow a path always to exist from the output to either the power source or ground. To achieve this, the set of all paths to the voltage source must be complement of the set of all paths to ground.

3. Existing System

A Comprehensive approach is used in the existing system for improving the efficiency of carry skip adder.The speed enhancement is achieved by applying the concatenation and incrementation schemes to the conventional carry skip adder. By combining the concatenation and incrementation method to the regular carry skip adder the power consumption of the adder is low. The structure is based on the combination of concatenation and the incrementation

methods with the Conv-CSKA structure, and hence, is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics [1]. The logic replaces 2:1 multiplexers by AOI/OAI compound gates as shown in Fig.2. [1].

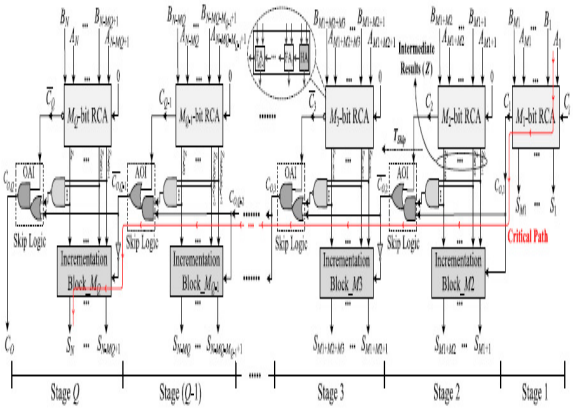

Fig 2. CI-CSKA Structure

The logic gates, which consists of fewer transistors, have lesser delay, area, and smaller power consumption compared with those of the 2:1 multiplexer. Note that, in this CI-CSKA structure, the carry that propagates through the skip logics, becomes complemented. Therefore, at the output of the even stages of skip logic, the complement of the carry is generated. The structure has a considerable smaller propagation delay with a slightly lower area compared with those of the conventional one. The power consumption of the CI-CSKA is a little more than that of the conventional one. Now, we describe the internal structure of the proposed CI-CSKA [1] shown in Fig.2 in more detail.

In addition, note that, the delay can be reducing considerably, by computing the carry output of eachstage, and the carry output of the incrementation block is not used. The incrementation block uses the intermediate results of the RCA block and the carry output of the previous stage to calculate the final summation of the stage. The critical path of the CI-CSKA structure, which contains three parts. The chain of the FAs is the first stage of these parts, the path of the skip logics is the second stage, and the incrementation block in the last stage. To calculate the delay of the skip logic, the average of the delays of the AOI and OAI gates, which are typically close to one another is used.

4. Proposed System

The proposed system uses a carry select adder structure with 32nm static CMOS technology. The carry select adder comprises of chain of full adders and multiplexers.A full adder adds binary numbers and calculate the values that carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and carry in; A and B are the operands, and carry in is a bit carried in from the next less significant stage. The full-adder is usually a component in a cascade of adders, bit wide binary numbers. In ripple carry adder each full adder inputs a carry in, which is the carry out of the full adder. Each full adder inputs a carry in, which is the carry out of the full adder.Each full adder requires three levels of logic.

The schematic diagram of full adder using static CMOS is shown in the Fig.3. The supply voltage is 1.2v.

Here A, B and carry in are the inputs, sum and carry out are the outputs. When all the inputs are low, the outputs are also low values. When the two inputs are, low and carry in is high, then the sum is high and the carry out is a low value. When all the inputs are high, the outputs are also high. The output sum is an EXOR between the input A and half adder sum output with B and Carry in inputs.

Thus, a full adder circuit can be executed with the help of two half adder circuits. The first half adder will be used to add A and B to obtain partial sum. The second half adder logic can be used to Carry in to the sum produced by the half adder to get the final sum output. If any of the half adder logic produces a carry, there will be an output carry. Thus, the carry out will be the OR function of the half adder carry outputs.

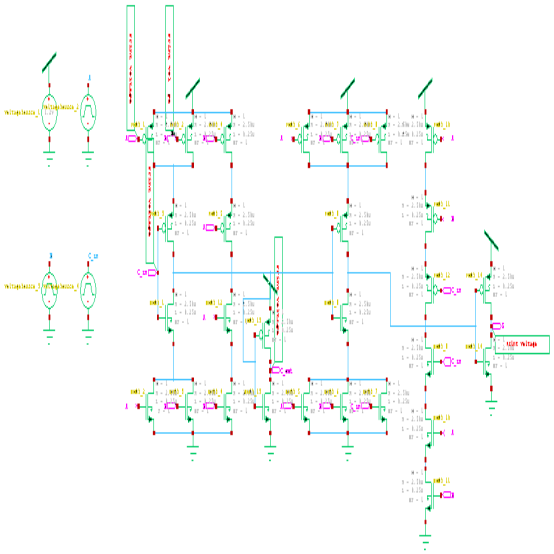

Fig 3. Schematic diagram of full adder

The schematic diagram of 2:1 multiplexer using the static CMOS technology is shown in the Fig.4.

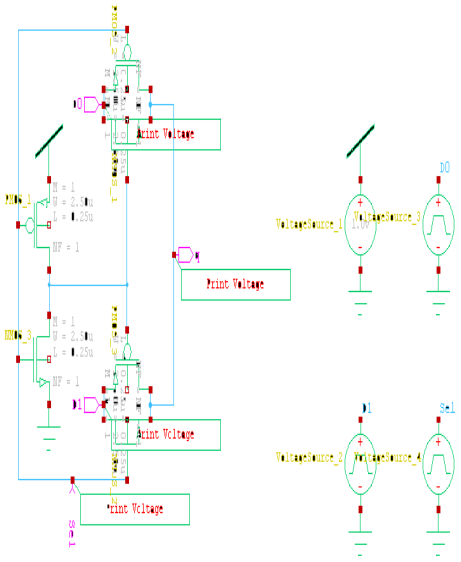

Fig 4. Schematic diagram of Multiplexer

The inputs are A and B. The output is represented as q. The main idea of multiplexing is to transmit two or more analog messages or digital signals concurrently over a single communication channel, thus sharing what might be an expensive resource. For example, in the telephone industry, a number of phone calls can be carried on a single wire. Another example is a home stereo system remote control that allows one to choose among the CD player, a DVD player, or cable TV. The sound systems having the digital output which carry several channels over a single fiber optic cable. In electronics, a multiplexer, or MUX, is a device that performs this multiplexing function by forwarding the selected input into a single channel.

The multiplexer is a device that selects one of the several analog or digital input signals and forwards the selected input in to a single line. A multiplexer of 2^ninputs has n select lines, which are used to select which input line to send to the output. When all the inputs are low, the output is also low. When any of the input is high, the output is also high. When all the inputs are high, the output is also high. Multiplexers are mainly used to increase the amount of data that can be send over the network within a certain amount of time and bandwidth. In this MUX one selection line (S) is used to select one of 2^1=2 input lines, D0 and D1, whose data is to be sent to the output (q).

5. Simulation Results

The simulation results of the proposed system are obtained using Tanner EDA. The simulated waveform of the full adder is shown in the Fig.5 below.

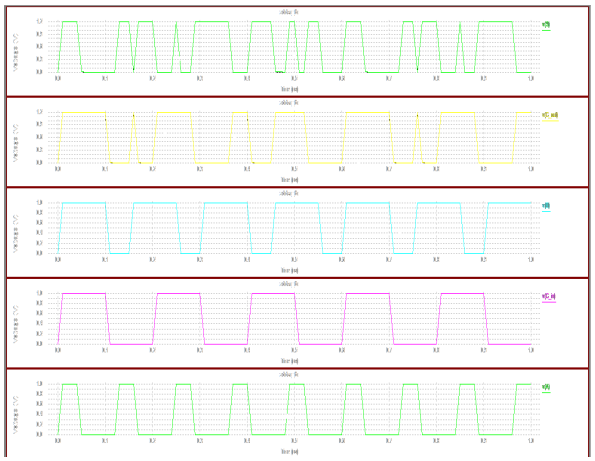

Fig 5. Simulated waveform of full adder

Here A, B and Carry in are the inputs. Sum and Carry out are the output. From the waveform, it is clear that the when all the inputs are a low value, the outputs are also a low value. Similarly, when all the inputs are high, the outputs are also high. Thus, a full adder circuit can be executed with the help of two half adder circuits. The first half adder will be used to add A and B to obtain partial sum. The second half adder logic can be used to Carry in to the sum produced by the half adder to get the final sum output.

The simulated waveform of 2:1 multiplexer is shown in the Fig.6.A multiplexer of 2^ninputs has n selection lines, that are used to select which of the input line is send to the output. Here D0 and D1 are inputs, S is the selection line. The output is represented by q. Based on the select line the inputs are selected. When all the inputs are low, the output is also low. When any of the input is high, the output is also high.

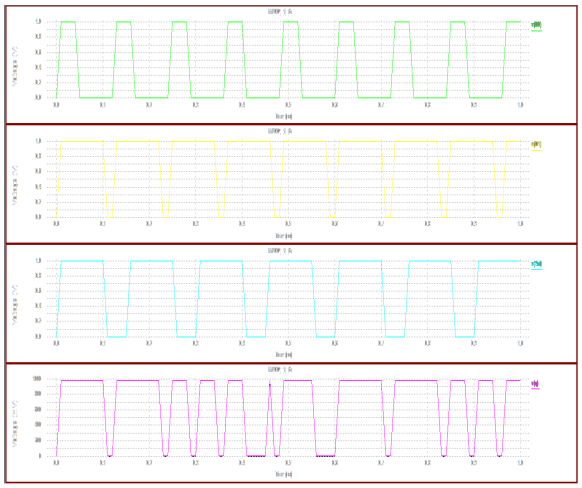

Fig 6. Simulated waveform of multiplexer

6. Power Consumption Analysis

The power consumption of full adder is obtained using Tanner as

```
* BEGIN NON-GRAPHICAL DATA

Power Results
vdd gnd from time 0 to 1e-006
Average power consumed -> 2.719811e-006 watts
Max power 1.310464e-004 at time 4.23554e-009
Min power 2.623779e-009 at time 6.2e-007


* END NON-GRAPHICAL DATA
*

* Parsing                    0.01 seconds
* Setup                      0.02 seconds
* DC operating point         0.03 seconds
* Transient Analysis         0.86 seconds
* Overhead                   1.39 seconds
* ------------------------------------
* Total                      2.30 seconds

* Simulation completed

* End of T-Spice output file
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From the analysis, the average power consumed by the full adder is 2.7µw. The maximum power obtained is 13.1mw and the minimum power is 2.62nw. Thus, the simulation results reveal that the full adder has low power consumption.

7. Conclusion

In future, a carry select adder is designed based on the concatenation and incrementation methods using static CMOS technology. The carry select adder consists of full adders and multiplexers. Here a full adder and multiplexer is designed using Tanner. The proposed system is simulated in 32nm CMOS technology at supply voltage of 1.2V. The power consumption of the full adder is 2.7µW.

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