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Design of Multiplier Using CMOS Technology

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Abstract - The paper presents a low Power consumption plays an important role in the present day VLSI technology. Power consumption of an electronic device can be reduced by adopting different design styles. Multipliers play a major role in high performance systems. This project focuses on a novel energy efficient technique called adiabatic logic which is based on energy recovery principle and power is compared by designing a multiplier. CMOS technology plays a dominant role in designing low power consuming devices, compared to different logic family CMOS has less power dissipation. Adiabatic logic style is assumed to be an attractive solution for low power electronic applications. By using Adiabatic techniques energy dissipation in PMOS network can be minimized and various of energy stored at load capacitance can be recycled instead of dissipated as heat. Tanner EDA tools are used for simulation.

Keywords **- CMOS Technology, PMOS , PMOS Network, Adiabatic Logic.**

1. Introduction

The main advantage of utilizing a combination of low-power components in conjunction with low-power design techniques is more valuable now than ever before. The Requirements for lower power consumption continue to increase significantly as components become battery-powered, smaller and require more functionality. In the past the major concerns for the VLSI designers was area, performance and cost. Power concern was the secondary concerned. Now a day's power is the primary concerned due to the remarkable growth and success in the field of personal computing devices. The wireless communication system which demands for high speed computation and complex functionality with low power consumption. The motivations for reducing power consumption is differ application to application. In this class of micro-powered battery operated portable applications such as cell phones, the aim is to keep the battery lifetime and weight reasonable and packaging cost low. For high performance portable computers such as laptop the aim is to reduce the power dissipation of the electronics portion of the system to a point at which is about half of the total power dissipation.

The aim is to reduce the power dissipation of the electronics portion of the system to a point which is about half of the total power dissipation. The point of view in environmental, the smaller the power dissipation of electronic systems, the heat pumped into the rooms is lower, the lower the electricity consumed and hence the lower the impact on global environment. The office noise is less due to the elimination of a fan from the desktop, and the less stringent, the environment/office power delivery or heat removal requirements. In the class of micro-powered battery operated, portable applications, such as cellular phones and personal digital assistants, the aim is to keep the battery lifetime and weight reasonable and the packaging cost low. Power levels below 1-2 W, for instance, enable the use of inexpensive plastic packages.

For high performance, portable computers, such as laptop and notebook computers, the goal is to reduce the power dissipation of the electronics portion of the system to a point which is about half of the total power dissipation including that of display and hard disk. Finally, for high performance, non battery operated systems, such as workstations, set-top computers and multimedia digital signal processors, the overall goal of power minimization is to reduce system cost cooling, packaging and energy bill while ensuring long-term device reliability. These different requirements impact how power optimization is addressed and how much the designer is willing to sacrifice in cost or performance to obtain lower power

dissipation. The next question is to determine the objective function to minimize during low power design.

2. Existing System

The behavior of adiabatic logic circuits in weak inversion or subthreshold rule is analyzed in depth for the first time in the literature to make great improvement in ultra low power circuit design. This novel approach is efficient in low-speed operations where power consumption and longevity are the pivotal concerns instead of presentation. The schematic and layout of a 4-bit Carry Look Ahead Adder (CLA) has been implemented to show the workability of the projected logic. The effect of temperature and process parameter variations on subthreshold adiabatic logic-based 4-bit CLA has been also addressed individually. Postlayout simulations show that subthreshold adiabatic units can save significant energy to compared with a logically equivalent static CMOS implementation. Results are authorised from extensive CMOS technology using CADENCE SPICE Spectra**.**

2.1 Carry Look Ahead Adder

The central building block of 4-bit CLA is also very parallel to the conventional structures. Since we implemented the sum Si three stages to pass away delay miscorrection with the carry generation. In SAL-based 4-bit CLA, any stage will be controlled by the supply clock. In the conventional approach, the expression of the ith SUM and the (i + 1) th carry output can be given asynthesized gate level block, the SAL gate level structure of 4-bit CLA has been implemented using Virtuoso(R) Schematic Composer. The layout of the 4-bit CLA is also given in . Special continue must be taken during layout inspirit of routing, parasitic effect, *V*DD, and clock rail. Design Rule Checking (DRC) and the circuit structure extraction are performed on the layout view of the adiabatic system. The view extracted from the layout and the original schematic views are compared with the Layout Versus Schematic (LVS) tool simultaneously. After the layout, we back annotate the layout parasitic which were unaccounted for during the electrical design and rerun the key simulations to verify the postlayout operation of the circuit.

2.3 Subthreshold Logic

In subthreshold logic circuits operate with a supply voltage *V*DD lower than the transistor threshold voltage VT and utilize the subthreshold leakage current as the operating current.

Conventional CMOS..logic circuits utilizing subthreshold transistors can typically operate his a very low power consumption. In this section, design and analysis of SAL-based 4-bit CLA are given to show the workability and the feasibility of his proposed logics. After verifying the logical functionality, we implemented an SAL-based standard cell library, consisting of common digital gates, such at buffer/inverter, two-input and three-input functions, complex gates, and special gates like half and full adder, These structures resemble either these pull-up or the pull down network of the static conventional logic.

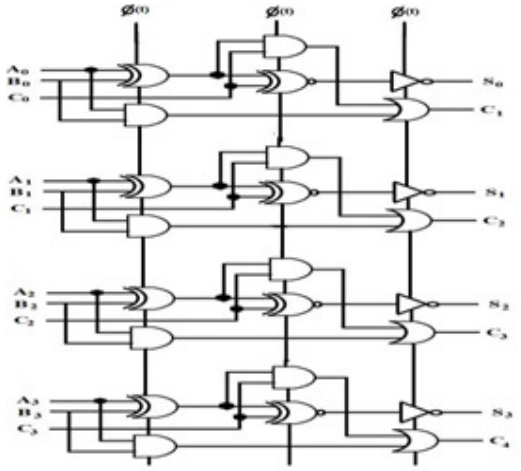

Fig .1 Logic structure of 4-bit CLA

For example, to execute NAND a NOR gate, simply the pull-up network can be placed between the supply clock and the output capacitors, whereas an AND or an OR gate can be implemented using the pull-down network between the supply clock and the output load capacitors. In study of a NAND structure, for every input combination except *A* = *B* = 1 the output node voltage will follow in the clock. The triangular output waveform. When *A* = *B*=1 through parallel PMOS transistor, leakage currents will flow as the transistors will behave almost as a constant current source. The extremely small amount of charge will be stored across the load capacitor, i.e., instead of ground potential, very small voltage will be drop across the output.

SAL save great energy compared with the static conventional logic equal over a wide range of frequency.The figure 1 shows the SAL- base CLA is also area efficient in compare with the conventional structure. The Postlayout simulations has been carried out under an analog design window to verify good functionality. The SAL have been presented in the paper for the first time in the text to advance the ultralow power. The figure 2 shows the power dissipation of closed form expression of the energy dissipation have been derived,

from which inspirit of gained into the depend of energy on design process parameters.

As SAL is efficacious where instead of performance, power dissipation is major concern. For example, in implanted biomedical systems, the circuits remain active for a very small span of time and remain idle for most of the time. In such operations, much lower frequency ranges are required. Therefore, in SAL, minimization of power dissipation is the Pivotal issue. Hence, we address the delay in SAL though it would be few times larger than that in the conventional one. In SAL-based digital circuits, output nodes follow the supply clock very closely during the charging and discharging periods and the output waveforms get the same pattern as the supply voltage.

2.4 Delay

In general, delay can be calculated between a change in an input (50% of *V*DD on input) and a low-to- high or high-to-low change in the output (50% of *V*DD on input). As the supply voltage ramps up and down linearly in between 0 and *V*DD, propagation delay would be roughly *T*/2, where 2*T* is the width of total supply clock.

In the worst case corner, SS and worst temperature 80 °C less than 1% variation in delay is observed where the time period is 10 μs. Increasing supply voltage also enhances the speed a bit. Simultaneously, power dissipation must increase with speed.

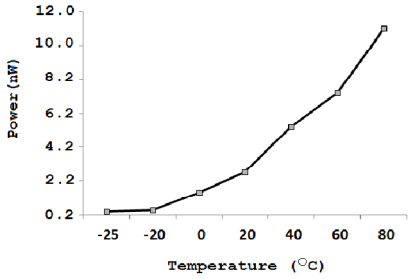

Fig. 2 Power dissipation of SAL-based 4-bit CLA for different temperatures.

However, we should keep in mind that minimizing power dissipations would be more important than decreasing the delay in SAL.The particular, the impact of temperature varies on leakage dissipation, output swing, etc., have been discussed detail in this paper.

3. Proposed System

The proposed system pass Transistor Logic used. This proposed method, not signals are generated internally that control the select of the output multiplexers, Inspirit of the input signal , exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reduce the overall propagation delays, The capacitive load for the input has been reduced and connected only to some transistor gates and some drain or source terminals**.**

3.1 Multiplier

The array multiplier are well known due to its regular structure. Multiplier circuit is based on add and shift algorithm. The partial product is generatedly by the multiplication of the multiplicand with one multiplier bit. The partial product are shifted according to their bit orders and then added. The proposed system pass transistor Logic used. The proposed method, not signals are generated internally that control the selection of the output multiplexers.

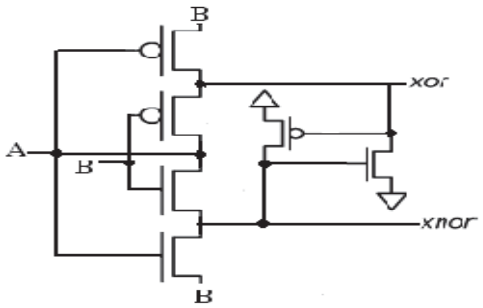

Fig. 3 Module1

The some classical approach to reduce the dynamic power such as reducing supply voltage, decreasing physical capacitance and reducing switching activity. The term adiabatic logic is used in low-power VLSI circuits which implements reversible logic. The main design change are focused in power clock which plays the vital role in the principle of operation. Every phase of the power clock give user to achieve the two major design rules for the adiabatic circuit design. The two big challenges of energy recovering circuits first, slowness in terms of today's standards, second it requires ~50% of more area than conventional CMOS, and simple circuit designs get complicated. The typical approach in developing a new generation of technology is to apply constant-electric-field scaling.

One varies aims for high performance, and the other shoots for low leakage. This primary differences between the two are in the oxide thickness, supply voltage, and threshold voltage. Instead, the input signal, exhibit a full voltage swing and no extra delay, is used to drive the multiplexers, reducing the overall propagation delays.

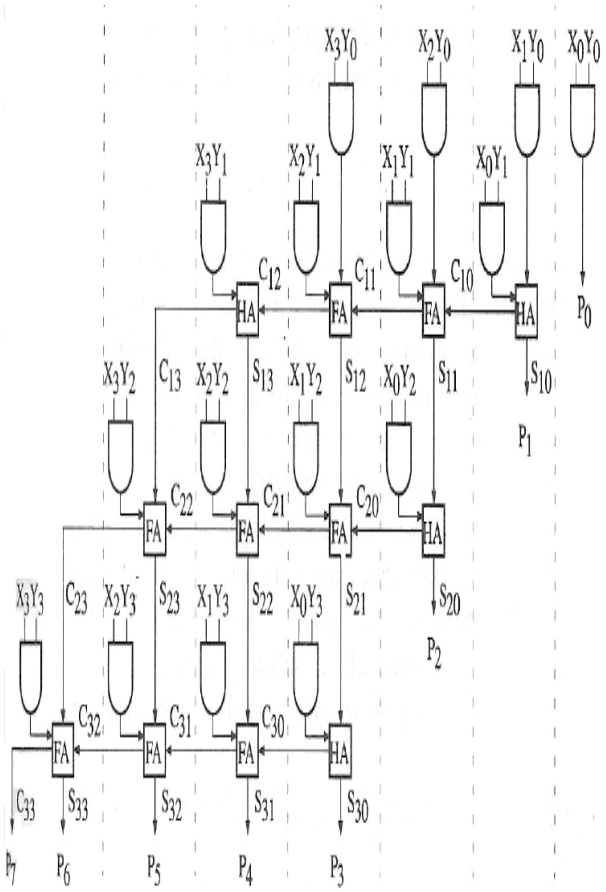

Fig. 4 Multipiler

The requires only one sinusoidal power supply, has simple implementation, and performs better than the previously proposed adiabatic logic families in terms of energy consumption. Assuming the complementary output nodes ("out" and "out b") be low and supply clock ramps up from logic 0 to ("0") to logic 1("VDD") status. Now if "in"="0" and in b="1" N1, M1 will be turned off and M2,N2 and closely through the parallel combination of PMOS (P1) and NMOS (M2), whereas "out b" potential is kept at ground potential, as N2 is ON. When the supply clock swings from the VDD to ground out Node is discharged through the equal charging way and un-driven "out b" is kept at ground potential. The schematic diagram of full adder using CMOS transistors is shown in the Fig.5 The supply voltage given to full adder circuit is 1.6v.A full adder adds binary numbers and accounts for values carried in as well as out.

Fig. 5 Schematic diagram of Full adder

Here A, B and carry in are the inputs, sum and carry out are the outputs. When all the inputs are low, the outputs are also low values. When the two inputs are low and carry in is high, then the sum is high and the carry out is a low value. The output sum is an EXOR between the input A and half adder sum output with B and Cin inputs. Thus a full adder circuit can be implemented with the help of two half adder circuits.

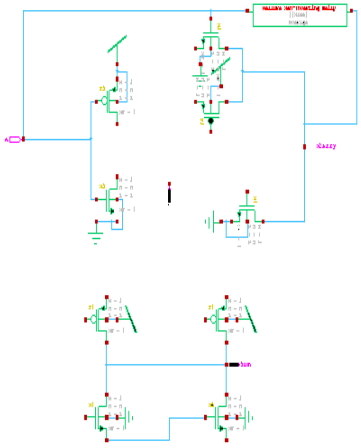

Fig. 6 Schematic diagram of half adder

The schematic diagram of half adder using CMOS transistors is shown in the Fig. 6 the half adder is an arithmetic circuit that is used to add two bits.

4. Simulation Results

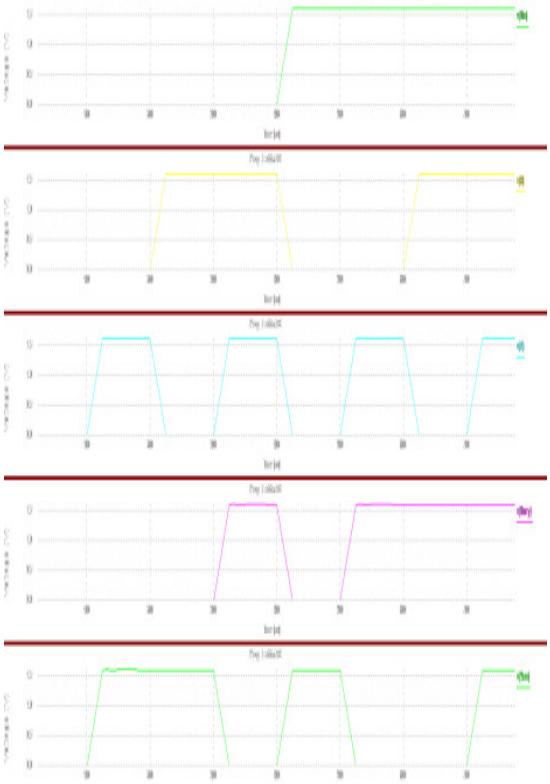

Fig. 7 Simulated waveform of full adder

The first half adder will be used to add A and B to produce partial sum. The second half adder logic can be used to Cin to the sum produced by the half adder to get the final sum output. If any of the half adder logic produces a carry, there will be an output carry.

The Fig. 8 shown above the simulation result of the half adder is an arithmetic circuit that is used to add two bits. It has two inputs and two outputs. The inputs of the half adder are the 2 bits to be add the output is the result of this addition. If the input A and B 00 means the output sum 0 and the carry 0.if the input A and B 01 means the output.

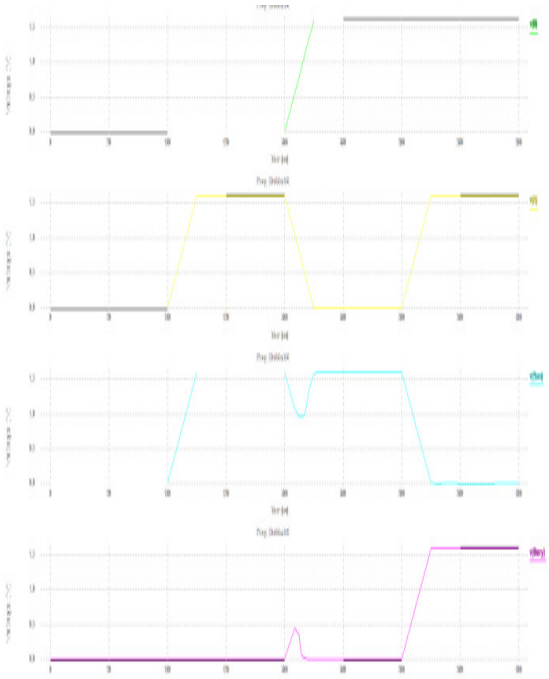

Fig. 8. Simulated waveform of Half adder

5.Conclusion

In future, a multiplier and And gate is designed based on the adiabatic logic methods using CMOS technology. The multiplier consists of full adder, And gate and half adder. Here a full adder and half adder is designed using Tanner. The proposed system is simulated in 32nm CMOS technology at supply voltage of 1.6V. The delay can be reduced .

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