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Design of Digital Circuits for ECG Data Acquisition System

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Abstract - Electrocardiogram (ECG) is the physical construal of the electrical behavior created by the heart muscles. The ECG signal consists of low amplitude voltage in the presence of high amplitude offset and noise. A new power-efficient electrocardiogram acquisition system uses a fully digital architecture to reduce the power consumption and delay time. This digital architecture is capable of operating with a low supply voltage of 0.3 V. In this architecture analog blocks such as low-noise amplifier (LNA) and filters are not used. A digital feedback loop is engaged to cancel the impact of the dc offset on the circuit, which eliminates the need of coupling capacitors. The circuit is implemented in 65nm CMOS process. The simulation results show that the front-end circuit of digital architecture consumes 0.22nW of power.

Keywords **- ECG, Offset, LNA, Digital, Acquisition, Amplitude, DCC Circuit.**

1. Introduction

Electrocardiogram (ECG) is a graphical recording of electrical activity of the heart over time. It is most recognized biological signal, and with non-invasive method; it is generally used for diagnosis of some diseases by inferring the signal. Cardiovascular diseases and its abnormalities alter the ECG wave shape; each portion of the ECG waveform carries information that is pertinent to the clinician in arriving at a proper diagnosis. The electrocardiograph signal is taken from a patient is generally get corrupted by external noises, hence it necessitating the require of a proper noise free ECG signal. A signal acquisition system, consist of several stages, as well as: signal acquisition though hardware and software instrumentation, noise or other characteristics filtering and processing for the extraction of information. Signal processing is performed in the vast majority of systems for ECG analysis and interpretation. It is used to extract several characteristic parameters. At present, biomedical signal processing have been towards quantitative or the objective analysis of physiological systems and phenomena via signal analysis. The objective of ECG signal processing is diverse and it comprises the improvement of measurement accuracy and reproducibility. ECG analysis concerns resting ECG elucidation, stress testing, ambulatory monitoring, or intensive care monitoring, which forms a basic set of algorithms that conditions the signal with respect to different types of noise and artifacts, detect heartbeats, haul out basic ECG measurements of wave amplitudes and durations, and compress the data for an efficient storage or transmission.

In all these applications, the biosignal is first preconditioned and converted to digital. A digital signal processor then processes the digital data for monitoring or diagnosis applications. Biomedical signal acquisition systems usually consist of a low-noise amplifier (LNA) , a bandpass filter, an analog sample-and-hold, and an analog-to-digital converter (ADC).Normally the analog devices consumes more amount of power and area. Digital systems play a remarkable role in today's life. They have important applications in virtually all fields of human activity and have a global influence on the performance of society. Digital describes electronic technology that generates, stores, and processes data in terms of two states: positive and non-positive. Positive is uttered or represented by the number 1 and the non-positive by the number 0. Thus, data transmitted or stored with digital technology is expressed as a string of 0's and 1's. Each of these state digits is referred to as a bit. People capture visual and auditory signals as a continuous stream. In contrast, digital devices estimate such information using ones and zeros. This rate of estimation is referred to as the “sampling rate,” which is united with the “bit depth,” or the amount of information included in every sample, to determine the accuracy of digital estimation. Information storage can be easier in digital systems than in analog ones. The noise-immunity of digital systems permits data to be stored and retrieved

without degradation. In analog system, noise from aging and wear degrade the information stored. In a digital system, as long as the total noise is below a certain level, the information can be recovered perfectly.

With the advancement of CMOS technology, the supply voltage is being reduced, which reduces the voltage headroom for analog block of an IC [1]. The technology scaling leads to the lower power consumption and higher performance in digital circuits. The parameters such as Signal-to-Noise Ratio (SNR), dynamic range and gain of the analog parts of an IC are negatively impacted. The power consumption in a signal processing system is often determined by dynamic range requirements. The dynamic range is a measure of the ratio between the largest signal that can be handled by the system without a significant distortion and the minimum detectable signal set by the input-referred noise.

Therefore, it is enviable to find new architectures in which more digital blocks are used. As can be seen, the amplifier; the only analog block that is used, consumes most of the power. Hence, if we can replace the amplifier with an appropriate digital block, the circuit will be more competent in terms of power. However, there are other issues that should be addressed before moving towards the fully digital implementation. Two of these issues are as follows [10].

1) Removing the DC Offset Voltage of Electrodes without Passive Elements
2) Providing a Solution for Anti-aliasing Filter.

2. Existing System

Biomedical signal acquisition systems [3] normally consist of a low-noise amplifier (LNA), a band-pass filter, an analog sample and hold, and an analog-to-digital converter (ADC). This analog block consumes more amount of power and area compared to the digital architecture. This digitally enhanced approach can helps to increase the flexibility of the system in removing unwanted interferences. Moreover, the digital calibration techniques can be used more easily.

2.1 Digital Front-End Architecture

In the existing system, with the advancement of CMOS technology, supply voltage is being reduced, which decreases the voltage headroom for analog block of an Integrated Circuit.

The block diagram of the system designed in [8] is shown in Fig.1. In this circuit, many of the functions that are normally implemented by analog blocks are performed by digital circuits. Using this digitally enhanced approach can help to increase the flexibility of the system in removing an unwanted interference.

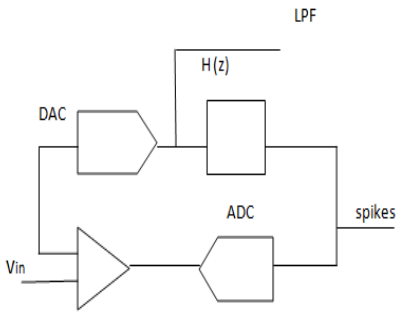

Fig.1 Mixed signal feedback architecture.

Eliminating the interferences at the input of the system, before extensive gain is applied, can relax the dynamic range requirements and minimize the supply voltage. This can lead to reduce the overall power consumption and area; both of which are crucial for implantable and multi-electrode systems [9]. This is achieved using mixed signal feedback and the digital blocks. Hence, it appears that the use of digital techniques in the implementation of these systems that can lead to a better performance and better compatibility with digital CMOS technology.

2.2 Offset Cancellation

The digital architecture is shown in Fig.2 It consists of an active electrode, two digital-to-current converters (DCCs), a moving average VTC (MA-VTC), a control logic block, a counter, and a demultiplexer.

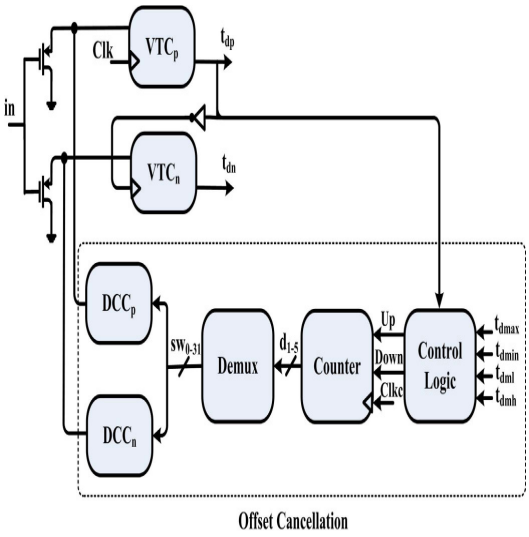

Fig.2 Block diagram of existing system

In this architecture, a new offset cancellation technique is used, in which offset cancellation is performed in two stages. First, the impact of the offset on the VTCs are eliminated, such that none of the VTCs are saturated.

This is achieved by a digital feedback loop and allows the circuit to take the value of the offset to digital output. In the second stage, the offset can be involved in the digital domain.

2.3 Active Electrode

Active electrode is electrodes that require no skin preparation. It is possible with preamplifier placed very close to the skin, inside electrode. High dry skin impedance can be omitted by using amplifier with very high input impedance. Another motive to use active electrodes is safety. Because the dry skin-electrode impedance is very high then the isolation barrier is much higher and a chance for an electrocution is much smaller than passive electrodes.

2.4 Voltage to Time Converter

In this digital implementation, the analog input voltage is converted to a measurable time via a VTC at the first stage [11]. The signal information is now in the delay of clock signal (CLK). The VTC should be designed in such a way that the small amplitude of the input voltage generates a large delay, linearly. In order to have the time-domain amplification and acceptable SNR, we have used 15 stages of positive VTC (VTC*p*) and 15 stages of negative VTC (VTC*n*). The delays versus input voltage of VTC*p* and VTC*n* are shown in Fig.3. As the input voltage becomes larger, the delay of VTC*p* increases, while the delay of VTC*n* decreases. The cascaded stages of VTCs form delay-line structures. A major advantage of the delay-line-based structure lies in its all-digital implementation. In addition, the delay line structures introduce time-domain amplification into the design. In particular, the input signal can be amplified in the time domain by simply extending the time window (using more VTC stages). This is in distinction to voltage amplification involving complicated analog amplifiers in the conventional systems [10]. The output of MA-VTC is the average of *V*in over a period of CLK signal. Actually, this circuit integrates signal in a time window *T*clk. Each VTC in the chain integrates the signal over a limited time period which depends on the delay of that VTC.

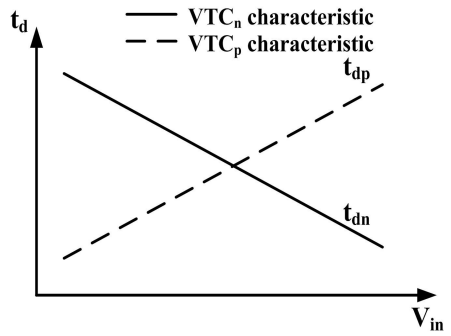

Fig. 3 VTC*n* and VTC*p* characteristics.

For example, the first VTC integrates the signal from the rising edge of the clock to the time equal to the delay of this VTC. The second VTC integrates the signal from the rising edge of the output of the first VTC over a time period determined by its delay. This happens for all the VTCs in the chain. The sum of these integration periods is equal to the clock period. Hence, the integration over this time window can be represented by

$$Y(Ts,t)=1/Ts\int vin(\tau)d\tau \quad (1)$$

Therefore, its impulse response is a rectangular pulse in the range of [0*, Ts]*

$$\delta(\tau)d\tau = u(t) - u(t - Ts) \quad (2)$$

Hence, its frequency response is a sinc function

$$H(j\omega) = 2\sin((Ts/2)\omega)/\omega Ts \quad (3)$$

In this way, the moving average filtering is embedded in the MA-VTC, preventing aliasing of the wideband noise.

2.5 Clock Frequency and Signal Recovery

VTC*p* and VTC*n* blocks are designed in such a way that the absolute slopes of their characteristic curves are equal. Hence, for any input voltage, we can write

$$tdp + tdn = t_{tot} = \text{Constant} \quad (4)$$

The delay time *tdp* (or *tdn*) of a VTC gate is supposed to be a linear function of its input voltage and is given by

$$tdp = \alpha V\text{inp} + \beta 1 \quad (5)$$

$$tdn = -\alpha V\text{inn} + \beta 2 \quad (6)$$

where *V*inp and *V*inn are the input voltage during the time interval that the clock pulse passes through VTC*p* and VTC*n*, respectively. In addition, α and $\beta 1,2$ are constants. The clock period, *T*clk, must be chosen such that for the maximum variation of the input *tdn* is not zero and is always measurable. Therefore, the clock period should be slightly more than t_{tot}.Hence

$$T\text{CLK} \geq tdp + tdn = \alpha(V\text{inp} - V\text{inn}) + \beta 1 + \beta 2. \quad (7)$$

The outputs of the digital front end are *tdP* and *tdn*. These delays are converted to two digital numbers (*DP* and *DN)* by two TDCs. The digital number corresponding to the input voltage, *D*in, can be obtained from

$$D\text{in} = Dp - Dn/2D\alpha + D\beta 2 - D\beta 1/2D\alpha \quad (8)$$

where $D\alpha$, $D\beta 1$, and $D\beta 2$ are digital numbers of α, $\beta 1$ and $\beta 2$, respectively.

2.6 Digital to Current Controller

The DCC generates a current proportional to its digital input and decreases/increases the input voltage of the VTC*p* and VTC*n*, each LSB of the DCC corresponds to 3.125 mV and this is the voltage that is added to/subtracted from the input in each step. This process will continue until the circuit goes into the *R*3 region. In this case, the offset value is on the tolerable range of the circuit, 5 mV. The transistors of the DCC are sized so that *V*inp and *V*inn are changed in a way that the impact of the offset at the input of the active electrode as well as that of the VTC and DCC blocks are cancelled. As a result, the delay of the VTC*p* block increases (decreases) and that the VTC*n* decreases (increases).This delay variation is sensed by the TCs in the control block and a new control bit is generated by the counter and Demux. This procedure is repeated until the operation of the VTC blocks goes back to region *R*3.

2.7 Control Logic

It is composed of TCs, AND and OR gates, and set-reset (SR) latches. An analog front end, for detecting the offset voltage, an analog voltage comparator should be used is shown in the Fig.4. In our design, the offset is detected by TCs, which are implemented by D flip-flops and are more power and area efficient compared with the analog voltage comparators. The outputs of the control logic circuit are the UP and DOWN signals, which control the up/down counter in the offset cancellation block. The counter in our design is implemented by NAND gates and JK flip-flops.

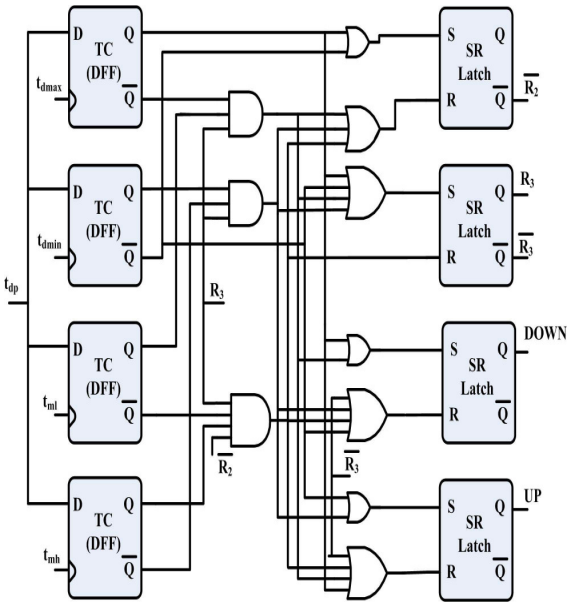

Fig.4 Schematic diagram of control logic

3. Proposed System

A new power-efficient ECG acquisition system that uses a fully digital architecture is proposed. In the system, active electrode, DCC and switch circuit is implemented in the 65nm CMOS technology to evaluate its performance. The supply voltage is 0.3 V, and the circuits are designed to operate in the sub- threshold region to reduce the power consumption. Each block of the system and its design challenges is discussed in the following sections.

3.1 Proposed System Block Diagram

The biosignal is generated from the active electrode is directly given to the two DCC blocks are used is shown in the Fig.5. These blocks are in charge of generating a current that depends on the 32-bit digital number (SW0 to SW31). The ECG signal acquisition system should be capable of rejecting the dc polarization voltage of the bio-potential electrodes, appearing as a dc offset at the input.

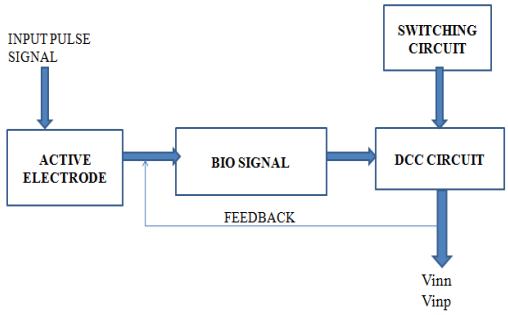

Fig.5 Proposed system block diagram.

This requires a High-Pass Filter (HPF) with a cutoff frequency <1 Hz. This filter requires large capacitors and on-chip implementation of such a filter is not efficient in terms of area. The impact of the offset is eliminated. This is achieved by a digital feedback loop and allows the circuit to take the value of the offset to the digital output.

3.2 Active Electrode

An active electrode is an electrode, in which some active elements are used to decrease the power line interference. However, the offset and the output resistance are worse. Since, in ECG applications, the most important limiting factor is the input noise of the system.

3.3 Digital to Current Converter

In the fully digital ECG front-end architecture of Fig.6 shows two DCC blocks are used. These blocks are in charge of generating a current that depends on the 32-bit

digital number (SW0 to SW31) at the output of the Demultiplexer. The DCC generates a current proportional to its digital input and decreases/increases the input voltage of the VTC*p* and VTC*n*, each LSB of the DCC corresponds to 3.125 mV and this is the voltage that is added to/subtracted from the input in each step. This process will continue until the circuit goes into the *R*3 region. In this case, the offset value is on the tolerable range of the circuit, (5 mV).The transistors of the DCC are sized so that *V*inp and *V*inn are changed in a way that the impact of the offset at the input of the active electrode as well as that of the VTC and DCC blocks are cancelled. To better understand the behavior of the DCC, assume that the offset at the input increases (decreases) leading to a rise (fall) in *V*inp and *V*inn. As a result, the delay of the VTC*p* block increases (decreases) and that the VTC*n* decreases (increases). As can be seen, at the beginning, the offset cancellation circuit is acting and setting the output of the DCCs and after this transition time the output signal is reliable.

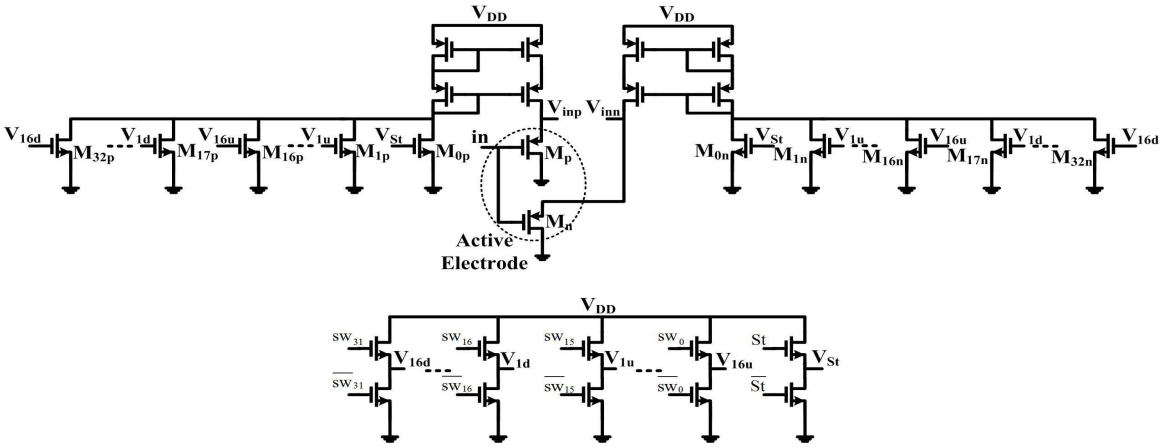

Fig.6 Structure of the current DCC

4. Simulation Results

The combined block of DCCs consists of two architecture DCCn and DCCp architecture ,each of this two architecture individually have 32 number of transistor in order to cancel out the DC offset. Here, the input is given in the two end of active electrode and the corresponding output is get from the two DCCs which is feedback to the active electrode. The NMOS gate terminal of the two DCCs architecture is connected to the switching circuit.

The switching circuit has two stages of NMOS, one is inverted and other is non inverted. These two stage common gate terminal is taken as input which is fed to the DCCs architecture. The input voltage given in this block is 5v and the output is nearly 0.5v is shown in the Fig.7.

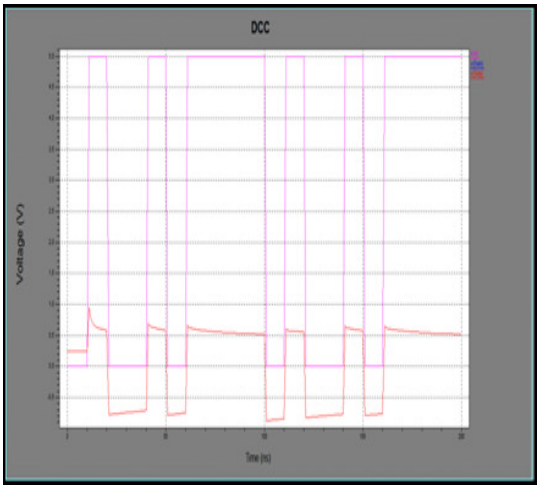

Fig.7 Output waveform of the DCC block.

5. Conclusion

In the expectation of the future dominance of digital CMOS technology, a fully digital front-end architecture for an ECG acquisition system was designed. In this system, active electrode, DCC and switching circuits

were implemented. The system has low power consumption, reduced delay time and less complexity. This digital architecture is simulated in 65nm CMOS technology at 0.3 V supply voltage. The simulated power consumption is 0.22nW their corresponding delay is -1.3071e-007.In future, digital architecture can be modified to accept an offset voltage larger than ±300 mV. In order to do this, the resolution of the DCC circuit and demultiplexer should be increased to 8 bits. A moving average mechanism embedded into the VTC of the front end eliminates the need for anti-aliasing filter.

References

[1] Maryam Zare and Mohammad Maymandi – Nejad , 'A fully digital front end architecture for ECG acquisition system with 0.5 V supply," IEEE Transaction on (VLSI) Systems, (2015), vol. 24, pp.256-265.

[2] Pieter Harpe ,Gao, Rainier van Dommele, Eugenio Cantatore and Arthur H. M. van Roermund, 'A 0.20 mm^2 3 nW Signal Acquisition IC for Miniature Sensor Nodes in 65 nm CMOS', IEEE J. Solid-State Circuits, vol. 51, no. 1,(2015), pp.240-248.

[3] Chih-Chan Tu and Tsung-Hsien Lin, 'Analog Front-End Amplifier for ECG Applications with Feed-Forward EOS Cancellation', IEEE on (VLSI-DAT), (2014), pp.1-4.

[4] Horng-Yuan Shih, Sheng-Kai Lin, and Po-Shun Liao, 'An 80× Analog-Implemented Time-Difference Amplifier for Delay-Line-Based Coarse-Fine Time-to-Digital Converters in 0.18-μm CMOS', IEEE (VLSI) Systems, vol. 23, (2014), pp.1528-153.

[5] Hyejung Kim, Sunyoung Kim and Nick Van Helleputte, 'A Configurable and Low-Power Mixed Signal SOC for Portable ECG Monitoring Applications', IEEE Biomedical Circuits And System, vol. 8, (2013), pp-257-267.

[6] Bo-Yu Shiu, Shuo-Wei Wang, Yuan-Sun Chu and Tsung-Heng Tsai, 'Low-Power Low-Noise ECG Acquisition System with DSP for Heart Disease Identification', IEEE Biomedical Circuits and System, (2013), pp-21-24.

[7] Rikky Muller, Simone Gambini, and Jan M.Rabaey, 'A 0.013 mm², 5 μ W, DC-Coupled Neural Signal Acquisition IC with 0.5 V Supply', IEEE J. Solid-State Circuits, vol. 47, no. 1, (2012) , pp.232-243.

[8] Tsung-Heng Tsai, Jia-Hua Hong, and Shuenn-Yuh Lee, 'Low-Power Analog Integrated Circuits for Wireless ECG Acquisition Systems', IEEE Information Technology In Biomedicine, vol. 16, no. 5, (2012), pp. 907-917 .

[9] J.L.Bohorquez,MarcusYip, A.P.Chandrakasan, J.L.Dawson, 'A biomedical sensor interface with a sinc filter and interference cancellation', IEEE J. Solid-State Circuits, vol. 46, no.4, (2011), pp.746-756.

[10] Hamidreza Rezaee-Dehsork, Nassim Ravanshad, Reza Lotf, Khalil Mafinezhad, and Sodagar A.M., 'Analysis and design of tunable amplifiers for implantable neural recording applications', IEEE J. Emerg. Sel. Topics Circuits Syst, vol. 1, no. 4, (2011), pp. 546–556.

[11] Q. Fan, F. Sebastiano, J. H. Huijsing, and K. A. A. Makinwa, 'A 1.8 μW 60 nV/$\sqrt{}$Hz capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes', IEEE J. Solid-State Circuits, vol. 46, no. 7, (2011),pp. 1534–1543.