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PWM-Based Multilevel Cascaded Inverters Under Unbalanced DC Sources

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Abstract - This paper proposes pulse width modulation technique to get balanenced line to line out put voltage. in linearly modulation range maximize the modulation indeex ,linearly varying out put voltage occurs. In the cascaded multilevel inverter(MLCI) operating under unbalanced dc link the linear modulation is reduced caused to voltage imbalance as voltage references increses. In order to analyze these effects, the voltage vector space for MLCI is evaluated in detail. From this analysis, the theory behind the output voltage imbalance is explained, and the maximum linear modulation range considering an unbalanced dc-link condition is evaluated. After that, a neutral voltage modulation strategy is proposed to achieve output voltage balancing as well as to extend the linear modulation range up to the maximum reachable point in theory. In the proposed method, too large of a dc-link imbalance precludes the balancing simulations and the experiments for a seven-level phase-shifted modulated MLCI for electric vehicle traction motor drive show that the proposed method is able to balance line-to-line output voltages as well as to maximize the linear modulation range under the unbalanced dc-link conditions.

Keywords **- Harmonic Injection, Multilevel Cascaded Inverters (MLCIs), Neutral Voltage Modulation (NVM), Phase-Shifted (PS) Modulation, Space Vector Pulsewidth Modulation (PWM) (SVPWM).**

1. Introduction

MULTILEVEL inverters enable the synthesis of a sinusoidal output voltage from several steps of voltages. For this reason, multilevel inverters have low *dv/dt* characteristics and generally have low harmonics in the output voltage and current. In addition, the switching of very high voltages can be achieved by stacking multilevel inverter modules [1]–[5]. Due to these advantages, multilevel inverters have been applied in various application fields [6]–[10]. Among various topologies for multilevel inverters, the multilevel cascaded inverter (MLCI) structure is one of the prominent topologies because of its simple structure for modularization and fault-tolerant capability. Therefore, MLCIs are used for many applications, such as dynamic voltage restorer, static synchronous compensator (STATCOM), high-voltage energy storage device, photovoltaic inverters, medium-voltage drives, electric vehicle (EV) traction drives, and so on [13]–[24]. In MLCI applications, a modulation strategy to generate gating signals is very crucial to achieve high-performance control. Regarding this issue, many studies have been conducted, and they are roughly categorized into multilevel selective harmonic elimination pulsewidth modulation (PWM) (SHEPWM), multilevel carrier-based PWM, and multilevel space vector PWM (SVPWM) methods [4].

Generally, a carrier-based PWM or SVPWM is preferred in applications such as motor drives [15], where dynamic properties are very important, whereas SHEPWM is preferred in some high-power static power conversion applications [11], [12]. In [25], an SVPWM method has been studied to cover the over modulation range in the multilevel inverter. To reduce the common-mode voltage, a multilevel SVPWM has been proposed in [26]. The series SVPWM method has been reported to easily implement SVPWM for the MLCI [27]. In [28], an SVPWM is proposed for hybrid inverters consisting of neutral point clamp and H-bridge inverters to improve output voltage quality and efficiency. As with two-level inverters, it is also possible to implement carrier-based SVPWMs which are equivalent to traditional SVPWMs by injecting a common offset voltage to the three-phase references [29]–[31]. In [29]– [31], some methods to calculate the offset voltages to achieve the optimal space vector switching sequence are addressed. The performances of a carrier-based PWM and an SVPWM are compared, and a PWM scheme is proposed to obtain an optimal output voltage in the multilevel inverter in [31].

On the other hand, MLCIs require separated dc links. Therefore, if there is one or more faults present in the dc links in each phase, or if the voltage magnitudes of the dc links are unequal, the output voltage of the MLCI can be unbalanced without proper compensation. To resolve this issue, some studies have been conducted. In [32], it is shown that the available modulation index is reduced under faulty conditions on switch modules in multilevel inverters, and compensation algorithms are proposed for phase-disposition PWM and phase-shifted (PS) PWM cases. For a STATCOM application, a zero sequence voltage to decouple a three-phase MLCI into three singlephase MLCIs is applied as well as zero average active power techniques to operate the MLCI under unbalanced source or load conditions [33]. Reference [34] explains why the optimum angles and modulation indexes are necessary to obtain maximum balanced load voltages in the MLCI undergoing a fault on switching modules.

A neutral voltage shifting technique has been introduced for balancing the state of charge in the MLCI-based battery energy storage system [35]. In [36], a duty cycle modification method has been proposed to compensate an output voltage imbalance caused by single-phase power fluctuations. Reference [37] has shown that a zero sequence component helps to obtain the maximum balanced output voltages in a fault condition. In [38], an offset voltage injection technique is studied to balance the output voltage of the MLCI, but the use of an integrator in the compensation method may reduce dynamic characteristics in applications such as EV motor drives.

Recently, the multilevel multiphase feedforward space vector modulation technique called MFFSVM is proposed to compensate the voltage imbalances in MLCIs [39], [45]. In this paper, a carrier-based PWM strategy to balance line to line output voltages and to maximize the linear modulation range where the output voltage can be linearly controlled in the MLCI operating under unbalanced dc-link conditions is proposed. In unbalanced dc-link conditions, the maximum synthesizable voltage in each phase is not uniform. Consequently, the linear modulation range is reduced, and a significant output voltage imbalance may occur as output voltage references increase. In order to analyze the imbalance effect, the voltage vector space for the MLCI is evaluated in detail.

From this analysis, the theory behind the output voltage imbalance is explained, and the maximum linear modulation range considering unbalanced dc sources is evaluated. After that, a neutral voltage modulation (NVM) strategy is proposed to achieve output voltage balancing as well as to extend the linear modulation range up to the maximum reachable point in theory. In the proposed method, the neutral voltage reference, which considers a zero sequence voltage to compensate the output voltage imbalance, and an offset voltage to extend the linear modulation range are easily obtained through simple arithmetic calculations. In the proposed method, too large of a dc-link imbalance precludes the output voltages from being balanced. This limitation is also discussed. In addition, a fault-tolerant operation is naturally covered, because the MLCI undergoing an unbalanced dc-link condition can be considered as an MLCI operating under a faulty condition on switch modules. Compared to the existing methods, the proposed strategy is very simple to implement, compensates the output voltage imbalance in real time, and maximizes the voltage utilization of the dc links. Therefore, if this scheme is applied to applications such as EV traction drive systems, the dynamic characteristics can be greatly improved.

This paper is organized as follows. In Section II, the voltage vector space for the one-by-three configuration MLCI is analyzed for a conceptual study. The proposed modulation strategy is addressed in Section III. In Sections IV and V, the simulations and the experimental results on the two-by-three MLCI are presented. Section VI concludes this paper.

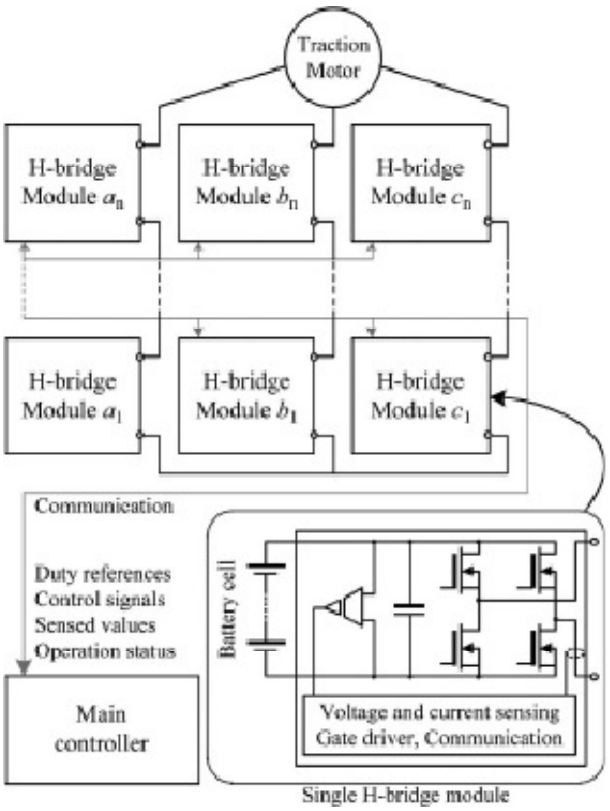

Fig. 1. MLCI-based inverter for EV traction drive.

2. System Configuration And Voltage Vector Space Analysis

2.1. Configuration of MLCI for EV Traction Motor Drive

Fig. 1 shows the EV traction motor drive system that is dealt with in this paper. In this configuration, various power ratings can be easily implemented by configuring the number of the single H-bridge modules according to a required specification such as a neighborhood EV, full-size sedan, and so on. Here, each H-bridge module incorporates voltage and current sensing circuitries, gate drivers, and communication interfaces between the module itself and the main controller. In addition, battery cells can be also included in the H-bridge module. The unipolar modulation technique is applied between two switching legs in the H-bridge module. Consequently, the effective switching frequency in each H-bridge module is twice the carrier frequency.

In addition to this, the well-known PS modulation technique is used to implement interleaving and multilevel operation [40]– [42]. Therefore, the effective switching frequency *f*sw in a phase is

$$f_{sw} = 2N \times f_c \qquad (1)$$

where N and fc represent the number of the H-bridge modules in each phase and the carrier frequency of PWM, respectively.

As an example, Fig. 2 shows the carriers for each module, the duty cycles in unipolar modulation, and the output voltage when $N = 2$.

2.2. Voltage Vector Space Analysis

When the dc-link voltage of a single H-bridge module is *V*dc, the output voltage *vpn* has three states, i.e., *V*dc, 0, and −*V*dc,

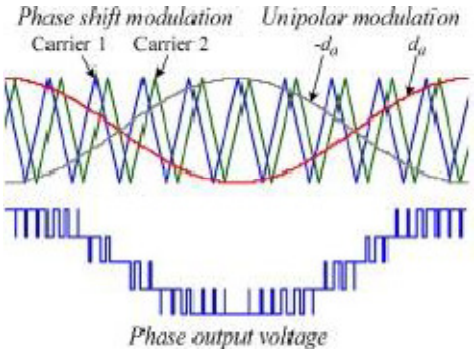

Fig. 2. Unipolar and phase shift modulation for single H-bridge module.

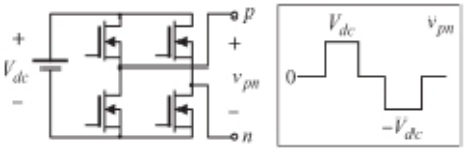

Fig. 3. Output voltage of a single H-bridge module.

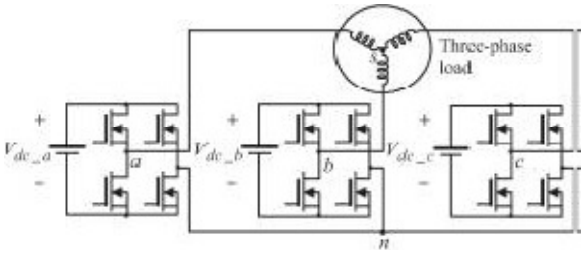

Fig. 4. One-by-three configuration MLCI.

as shown in Fig. 3. By adopting the concept of a switching function, it can be represented as

$$v_{pn} = S_p V_{dc}$$
$$S_p \in \{-1, 0, 1\}_{p=a,b,or,c} \qquad (2)$$

where Sp is a switching function and p can be replaced with a, b, or c, which represent the phases.

Fig. 4 shows a simple one-by-three configuration MLCI. For voltage vector space analysis, the main concept is derived from this simple topology, and then, it is expanded to more levels. In Fig. 4, there are two neutral points s and n in the MLCI. Here, the voltage between the output point of each phase and the neutral point n is defined as the pole voltage. The pole voltages are represented as *van*, *vbn*, and *vcn*. The voltage between the output point of each phase and the load side neutral point s is specified as the phase voltage. The phase voltages include *vas*, *vbs*, and *vc s*. By using this concept, the voltage between the two neutral points is defined as *vsn* and can be written as,

$$v_{sn} = -v_{as} + v_{an} = -v_{bs} + v_{bn} = -v_{cs} + v_{cn}. \qquad (3)$$

By using the condition that the sum of all phase voltages is zero because the load does not have a neutral line, *vsn* is rewritten as,

$$v_{sn} = \frac{1}{3}(v_{an} + v_{bn} + v_{cn}). \qquad (4)$$

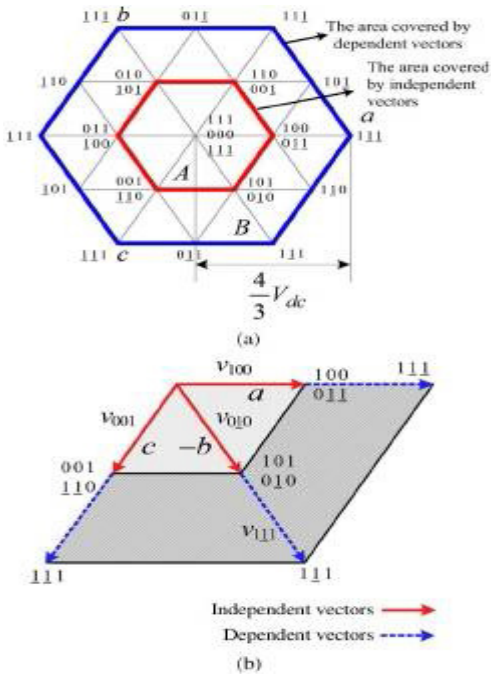

Fig. 5. Voltage vector space of one-by-three configuration MLCI.

By substituting (4) into (3), the phase voltage of each phase is represented as follows by using the relationship defined in (2):

$$v_{as} = 2/3S_aV_{dc\_a} - 1/3S_bV_{dc\_b} - 1/3S_cV_{dc\_}$$

$$v_{bs} = -1/3S_aV_{dc\_a} + 2/3S_bV_{dc\_b} - 1/3S_cV_{dc\_c}$$

$$v_{cs} = -1/3S_aV_{dc\_a} - 1/3S_bV_{dc\_b} + 2/3S_cV_{dc\_c}. \quad (5)$$

If the magnitudes of three dc links are balanced so that *V*dc_*a*, *V*dc_*b*, and *V*dc_*c* have the same value *V*dc, the voltage vector space in $\alpha-\beta$ coordinates is defined in Fig. 5(a) by using (5).

In the figure, underbars indicate that the switching function has the value of −1. A part of the hexagon in Fig. 5(a) is shown in Fig. 5(b). In this figure, the vectors *v*010 and *v*111 are placed at the same reference axis, phase *b*. However, the constituents of those vectors are different. For *v*010, this vector can be synthesized without the other two phases' assistance. However, *v*111 cannot be produced without other vectors according to (5). From this, let the vectors which do not require other two phases' assistance to be defined as "the independent vectors." Similarly, the vectors which require other phases' support are defined as "the dependent vectors." According to these definitions, *v*100, *v*001, and *v*010 are the independent vectors, while *v*111, *v*111, and *v*111 are the dependent vectors in Fig. 5(b). Fig. 5(a) also compares the regions that can be composed by the independent

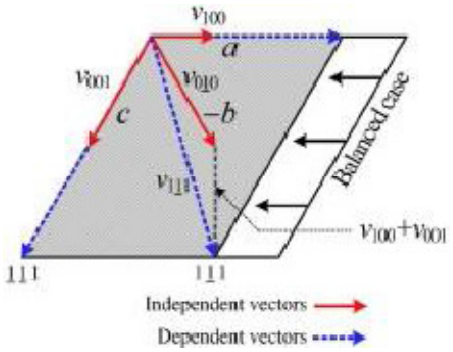

Fig. 6. Voltage vector space in an unbalanced dc-link condition.

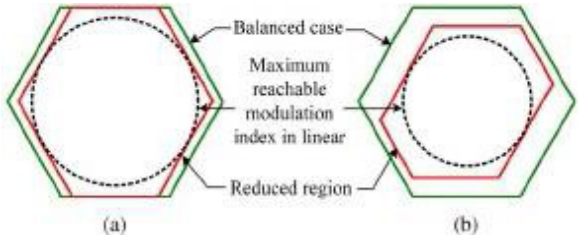

Fig. 7. Comparison of the voltage vector space under different dc-link ratios

and the dependent vectors. Unlike traditional three-phase half bridge inverters, the independent vectors can be fully applied in a switching period because the dc links in each of the three phases are separated in the given system. It should be noted that the maximum voltage is decided by the dependent vectors in the entire voltage vector space. Now, let us consider the case when a three-phase load is supplied by unequal dc links. Fig. 6 shows an extremely unbalanced case where *V*dc_*a* is half of the others. If *V*dc_*a* decreases, the magnitudes of the independent vectors in phase *a* are also reduced.

As a result, the magnitude of *v*100 isdecreased. Here, the phase angle of *v*111,which is the sum of 010, *v*100, and *v*001, is no longer matched with the angle of the independent vectors in phase *b* from the figure. As shown in the figure, if the magnitudes of the independent vectors are reduced, the available voltage vector space is also reduced, and the angles of the dependent vectors are no longer multiples of 60◦. Using these properties, the voltage vector spaces in two different cases are compared in Fig. 7. In Fig. 7(a), *V*dc_*a* has a lower value than the others. In Fig. 7(b), all three dc links have different voltages. As it can be seen in Fig. 7, the original shape of the hexagon is distorted in both cases. This means that the trajectory of the maximum output voltage vector in the $\alpha-\beta$ coordinates is also distorted

according to the shape of the hexagon in each. On the other hand, the magnitude of the maximum modulation index in the linear modulation range in a given hexagon corresponds to the radius of the inner circle which is inscribed in the hexagon. As shown in Fig. 7, the radius is changed as the hexagon distorts, and the achievable linear modulation range is also altered. Here, the maximum amplitude of the phase voltage *V*ph_ max in the linear modulation range is defined as

$$V_{ph\_max} = V_m \left(V_{dc\_max} \frac{\sqrt{3}}{2} \left(\frac{4}{3} - \frac{2}{3} \frac{V_{dc\_max} - V_{dc\_mid}}{V_{dc\_max}} - \frac{2}{3} \frac{V_{dc\_max} - V_{dc\_min}}{V_{dc\_max}} \right) \right) \quad (6)$$

Voltage limitation from the medium dc link

Voltage limitation from the minimum dc link

where *V*dc_ max, *V*dc_mid, and *V*dc_ min represent the maximum, medium, and minimum voltages among the dc links. In fact, (6) can be simplified as

$$V_{ph\_max} = \frac{V_{dc\_mid} + V_{dc\_min}}{\sqrt{3}}. \quad (7)$$

It should be noted that *V*ph_ max is the maximum synthesizable voltage in the linear modulation range in the MLCI undergoing unbalanced dc-link conditions. From (7), it can be recognized that *V*ph_ max is determined by *V*dc_mid and *V*dc_ min. If all dc links are well balanced so that *V*dc_mid and *V*dc_ min have identical values, (7) is rewritten as

$$V_{ph\_max} = \sqrt{2}/3 \; V_{dc} \quad (8)$$

This is exactly double the maximum synthesizable voltage in the linear modulation range of a traditional three-phase halfbridge inverter. In fact, the inverter in Fig. 4 is considered as a three-phase full-bridge inverter which is fed by independent dc links. To extend the proposed approach to the multistage

$$V_{dc\_p} = \sum_{j=1}^{N} V_{dc\_p(j)p=a,b,or\,c} \quad (9)$$

MLCI using PS modulation, the total dc-link voltage per phase is represented as where *p* represents a certain phase among phases *a*, *b*, and *c*, *N* is the number of the power stage modules in each phase, and *j* represents the index of a power stage module in each phase.In the multistage MLCI, (9) is utilized to obtain *V*dc_ max, *V*dc_mid, and *V*dc_ min. After that, (7) is still applied.

3. Proposed Modulation Technique

In Section II, the maximum synthesizable voltage in the linear modulation range was evaluated under the unbalanced dc links. In this section, a method is proposed to realize the maximum modulation index in the linear modulation range under these conditions.

3.1. Traditional Offset Voltage Injection Method

The offset voltage injection scheme is a popular technique in three-phase half-bridge inverter applications. The theory behind this is that an offset voltage is incorporated with phase voltage

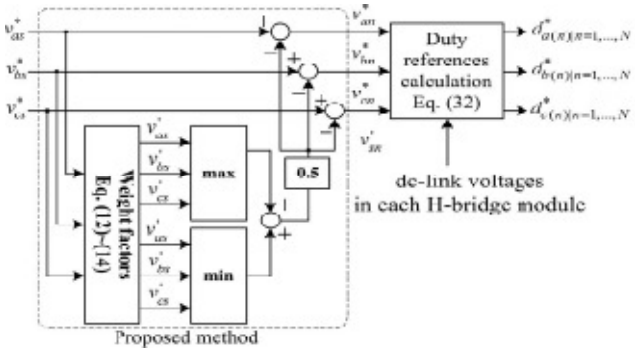

Fig. 8. Implementation of the NVM method.

references to implement various PWM schemes in carrier-based PWM by using the fact that line-to-line voltages are applied to a three-phase load [43], [44]. For example, the offset voltage*vsn* is injected to the phase voltage references*vas*, *vbs*, and *vcs*to implement carrier-based SVPWM as in

$$v_{sn}^* = \frac{v_{max}^* + v_{min}^*}{2} \qquad v_{max}^* = \max(v_{as}^*, v_{bs}^*, v_{cs}^*)$$
$$v_{min}^* = \min(v_{as}^*, v_{bs}^*, v_{cs}^*). \quad (10)$$

Then, the pole voltage references *van*, *vbn*, and *vcn*, which will be converted to PWM duty references, are

$$v_{an}^* = v_{as}^* - v_{sn}^* \quad v_{bn}^* = v_{bs}^* - v_{sn}^* \quad v_{cn}^* = v_{cs}^* - v_{sn}^* \quad (11)$$

However, the aforementioned technique may not maximize the linear modulation range in MLCI undergoing unbalanced dc-link conditions.

$$K_w = \frac{V_{dc\_mid} + V_{dc\_min}}{2}. \quad (12)$$

By using (12), the weight factors are calculated as

$$K_{w\_a} = \frac{K_w}{V_{dc\_a}} \qquad K_{w\_b} = \frac{K_w}{V_{dc\_b}} \qquad K_{w\_c} = \frac{K_w}{V_{dc\_c}} \qquad (13)$$

where *Kw_a*, *Kw_b*, and *Kw_c* represent the weight factors for phases *a*, *b*, and *c*, respectively. Next, the weight factors are multiplied by the phase voltage references, and the new references *vas*, *vbs*, and *vc s* are obtained as

$$v_{as} = K_{w\_a} v_{as}^{***} \qquad v_{bs} = K_{w\_b} v_{bs} \qquad v_{cs} = K_{w\_c} v_{cs}. \qquad (14)$$

It should be noted that, depending on dc-link conditions, the sum of *vas*, *vbs*, and *vc s* may not be zero. By using these components, the injected voltage *vsn* and the pole voltage references are given as

$$v_{\max} = \max(v_{as}, v_{bs}, v_{cs}) \qquad v_{\min} = \min(v_{as}, v_{bs}, v_{cs})$$

$$v_{sn} = \frac{v_{\max} + v_{\min}}{2} \qquad \begin{bmatrix} v_{an}^{**} \\ v_{bn}^{**} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} v_{as}^{**} - v_{sn} \\ v_{bs} - v_{sn} \\ v_{cs} - v_{sn} \end{bmatrix}. \qquad (15)$$

From (15), the line-to-line voltages across each phase of the load are represented as

$$\begin{bmatrix} v_{ab}^{**} \\ v_{bc}^{**} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} v_{an}^{**} - v_{bn} \\ v_{bn} - v_{cn} \\ v_{cn} - v_{an} \end{bmatrix} = \begin{bmatrix} v_{as}^{**} - v_{sn} - v_{bs} + v_{sn} \\ v_{bs} - v_{sn} - v_{cs} + v_{sn} \\ v_{cs} - v_{sn} - v_{as} + v_{sn} \end{bmatrix}$$

$$= \begin{bmatrix} v_{as}^{**} - v_{bs} \\ v_{bs}^{**} - v_{cs} \\ v_{cs} - v_{as} \end{bmatrix}. \qquad (16)$$

As it can be seen in (16), *vsn* does not appear in the line-toline voltages, and it is still considered as a hidden freedom of voltage modulation. Now, let us consider the role of the weight factors *Kw_a*, *Kw_b*, and *Kw_c*, which are inversely proportional to the corresponding dc-link voltage. For convenience, let us assume that the magnitudes of the dc-link voltage are under the following relationship:

$$V_{dc\_a} < V_{dc\_b} < V_{dc\_c}. \qquad (17)$$

Then, from (13) and (17)

$$K_{w\_a} > K_{w\_b} > K_{w\_c} \qquad K_{w\_a} > 1$$
$$K_{w\_b}, K_{w\_c} < 1. \qquad (18)$$

Equation (18) gives

$$|v_{as}| > |v_{as}^{**}| \qquad |v_{bs}| < |v_{bs}| \qquad |v_{cs}| < |v_{cs}|. \qquad (19)$$

From (15) and (19), it can be recognized that, if *vas*, whose dc-link voltage is less than the others, is corresponding to *v*max or *v*min, the absolute value of *vsn* is greater than *vsn* in (10).

On the other hand, the final pole voltage references *van*, *vbn*, and *vcn* are calculated by subtracting *vsn* from the original phase voltage references *vas*, *vbs*, and *vc s* as in (15). From this reasoning, in this example, it is supposed that, if *vas* is corre- sponding to *v*max, then the final pole voltage references *van*, *vbn*, and *vcn* are less than the original pole voltage references

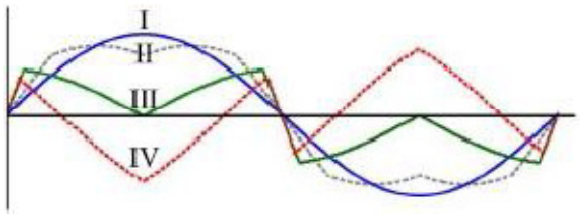

Fig. 9. Comparison of modulated waveforms

Which are not considering *vsn* but *vsn*. On the contrary, if *vcs* is *v*max, then the final pole voltage references are greater than the original pole voltage references. By using this principle, the proposed method reduces the portion of the phase whose dc-link voltage is smaller than the others and increases the utilization of the phase in which the dc-link voltage is greater than those of the other phases. However, as it can be seen in (16), *vsn* does not affect the line-to-line voltages. Therefore, the line-to-line voltage is the same as the one derived from the original phase voltage reference. From this analysis, the proposed method enables the maximum synthesizable modulation index in the linear modulation range under the unbalanced dc-link conditions to be achieved. In addition to this, if all of the dc-link voltages are well balanced so that *V*dc_*a*, *V*dc_*b*, and *V*dc_*c* are equal to *V*dc

$$V_{dc\_mid} = V_{dc\_min} = V_{dc}. \qquad (20)$$

By substituting (20) into (12)–(14)

$$K_w = \frac{V_{dc\_mid} + V_{dc\_min}}{2} = V_{dc}$$
$$K_{w\_a} = K_{w\_b} = K_{w\_c} = 1$$
$$v_{as} = v_{as}^{**} \qquad v_{bs} = v_{bs}^{**} \qquad v_{cs} = v_{cs}^{**}. \qquad (21)$$

Equation (21) shows that the proposed method gives the same voltage references as the traditional method under balanced dc-link conditions.

3.2. Constraints of the Proposed Method

In this section, the limitation of how unbalanced dc links can be while still being compensated by the proposed method is evaluated. Fig. 9 shows the modulated voltage waveforms with different modulation methods and dc-link conditions. In the figure, cases I and II show the results of traditional sinusoidal PWM (SPWM) and carrier-based SVPWM, while cases III and IV illustrate the waveforms of the proposed method with different ratios of dc-link voltages. The fundamental idea to examine the limitation of the proposed method is to evaluate what conditions bring the different polarities between the original voltage reference and the modified voltage reference by using the proposed method. In Fig. 9, the vertices at $\pi/2$ and $3\pi/2$ rad almost come in contact with, but do not cross, the zero point.

However, the directions of the vertices are opposite the original phase voltage reference in case IV. This means that an excessive and unnecessary voltage is injected into the system. As a result,

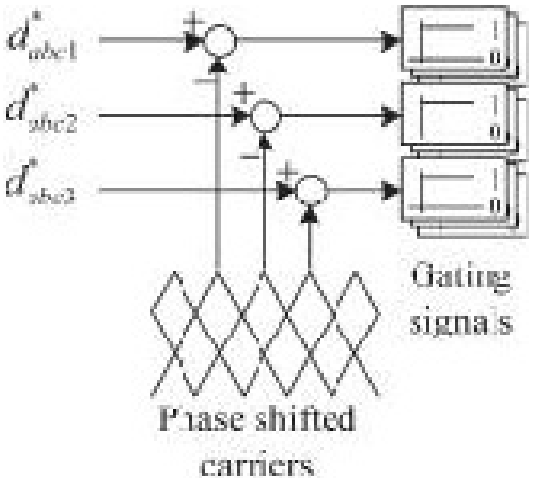

Fig. 10. Comparison of the duty references and the carriers.

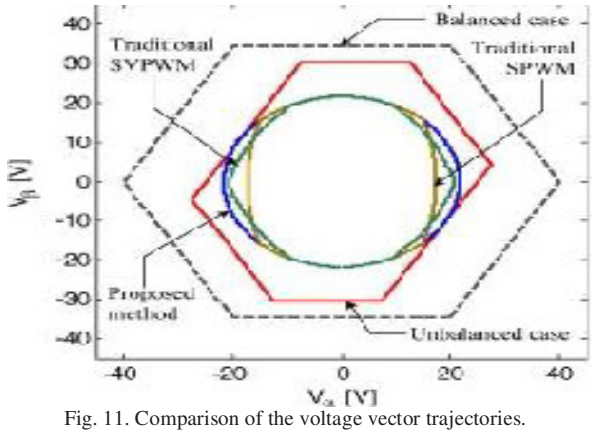

Fig. 11. Comparison of the voltage vector trajectories.

the maximum linear modulation range is reduced, and the line to- line voltage may be distorted. With this basic concept, it is assumed that a phase which has the lowest dc-link voltage commands *v*max and a phase which has the highest dc-link voltage commands *v*min to examine a worst case situation.

From (14) and (15), the following equations can be established:

$$V_{max} = \frac{V_{dc\_mid} + V_{dc\_min}}{2V_{dc\_min}} V^*_{max}$$

$$V_{min} = \frac{V_{dc\_mid} + V_{dc\_min}}{2V_{dc\_max}} V^*_{min}$$

$$V_{sn} = \frac{V_{max} + V_{min}}{2}. \qquad (22)$$

By using (22), the pole voltage reference which is considered as the worst case is

$$V^*_{max\_n} = V_{max} - \frac{V_{max} + V_{min}}{2}. \qquad (23)$$

By substituting (22) into (23), we have

$$V^*_{max\_n} = \left(1 - \frac{V_{dc\_mid} - V_{dc\_min}}{4V_{dc\_min}}\right) V_{max} - \frac{V_{dc\_mid} + V_{dc\_min}}{4V_{dc\_max}} V_{min}. \qquad (24)$$

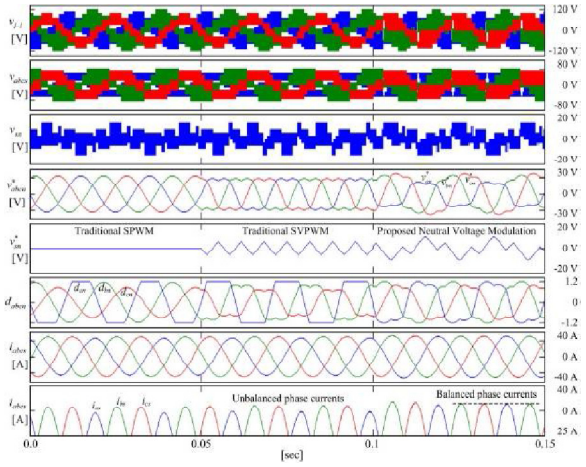

Fig. 12. Simulation result of traditional SPWM, traditional SVPWM, and the proposed method.

Fig. 12. Simulation result of traditional SPWM, traditional SVPWM, and the proposed method. Unless all three-phase voltage references are not zero simultaneously, near a positive peak of the original voltage reference, the

sufficient condition which guarantees the same polarity between *v*max and *v*min is established as follows,

$$v_{max\_n}^{*} > 0 \qquad v_{max}^{*} > 0 \qquad v_{min}^{*} < 0. \qquad (25)$$

By substituting (24) into the first condition in (25), the following condition can be written:

$$k_1 v_{max}^{*} > k_2 v_{min}^{*} \qquad k_1 = 1 - \frac{V_{dc\_mid} + V_{dc\_min}}{4V_{dc\_min}}$$

$$k_2 = \frac{V_{dc\_mid} - V_{dc\_min}}{4V_{dc\_max}}. \qquad (26)$$

Here, it is obvious that $k2$ is always positive. Therefore, as long as $k1$ is positive, the condition (26) is always satisfied, and $k1$can be rearranged as follows:

$4V_{dc\_min}$ (27)

Equation (28) is then directly obtained from (27) to ensure that $k1$ will always be positive

$$V_{dc\_min} > \frac{1}{3} V_{dc\_mid}. \qquad (28)$$

Note that (28) is a sufficient condition to meet the conditions in (25) so that the proposed method can be applied. However, even if (28) is not satisfied so that $k1$ is negative, there still is a chance to apply the proposed method. To deal with this situation, let us consider the relationship between *v*max and *v*min as follows at a positive peak point:

$$v_{max}^{*} = -2v_{min}^{*}. \qquad (29)$$

By substituting (29) into (26), we have

$$-2k_1 > k_2. \qquad (30)$$

Since $k1$ is negative in this case, the following condition is derived from (30);

$$|k_1| < \frac{k_2}{2}. \qquad (31)$$

If the relationship between $k1$ and $k2$ is established as in (31), even if the provision in (28) is broken, the conditions in (25) are satisfied so that the proposed method can be still effective.

Let us recall Fig. 9 again here. In the figure, the values of $|k1|$ and $k2/2$ for case III are evaluated as 0.1591 and 0.1593, respectively. Although the difference between the two values

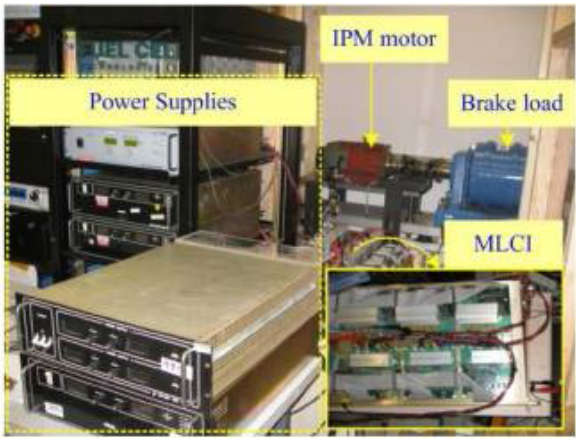

Fig. 13. Photograph of the experimental setup.

$$k_1 = \frac{3V_{dc\_min} - V_{dc\_mid}}{}$$

the values of $|k1|$ and $k2/2$ are calculated as 0.5 and 0.3, respectively. In contrast to case III, (31) is no longer satisfied, and the directions of the vertices are opposite, as explained previously. From the analysis in this section, both the methods in (28) and (31) are successfully able to judge the availability of the proposed method. In terms of accuracy, the latter may give better results. However, in practice, the former may be useful to judge the operation of the proposed method because it is already dealing with an extremely worst case on its own and the calculation in real time is much simpler than (31).

3.3. Duty Calculation

In Fig. 8, the final voltage references are entered to the duty reference calculation block. In this block, the duty references of each H-bridge module are calculated as follows

$$d_{a1}^{*} = d_{a2}^{*} = \cdots = d_{aN}^{*} = \frac{v_{an}^{*}}{V_{dc\_a}}$$

$$d_{b1}^{*} = d_{b2}^{*} = \cdots = d_{bN}^{*} = \frac{v_{bn}^{*}}{V_{dc\_b}}$$

$$d_{c1}^{*} = d_{c2}^{*} = \cdots = d_{cN}^{*} = \frac{v_{cn}^{*}}{V_{dc\_c}}. \qquad (32)$$

The calculated duty references are compared to PS carriers to generate gating signals, as shown in Fig. 10. It should be noted that the duty references for each H-bridge in each phase are shared in the PS modulation.

4. Simulation

A simple one-by-three configuration MLCI model is built in Matlab Simulink. The three-phase *RL* load with $R = 0.1\ \Omega$ and $L = 1$ mH is employed. The dc-link voltages for each phase are $V\text{dc}\_a = 0.5 \times 30$ V, $V\text{dc}\_b = 0.75 \times 30$ V, and $V\text{dc}\_c = 30$ V.

From (7), the maximum synthesizable phase voltage in linear is

$$V_{ph\_max} = ((0.75*30)+(0.5*30))/3 = 21.65\ \text{V}. \quad (33)$$

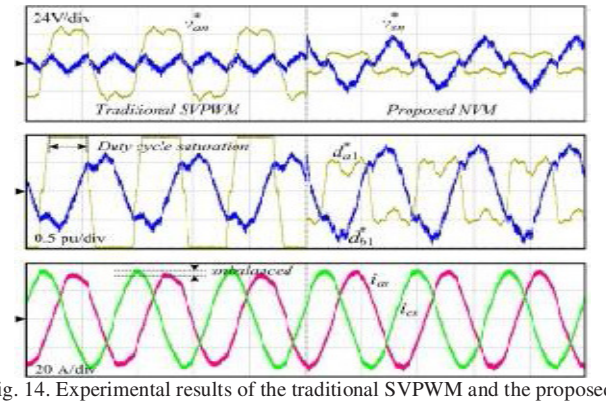

Fig. 14. Experimental results of the traditional SVPWM and the proposed NVM strategies (50 ms/div).

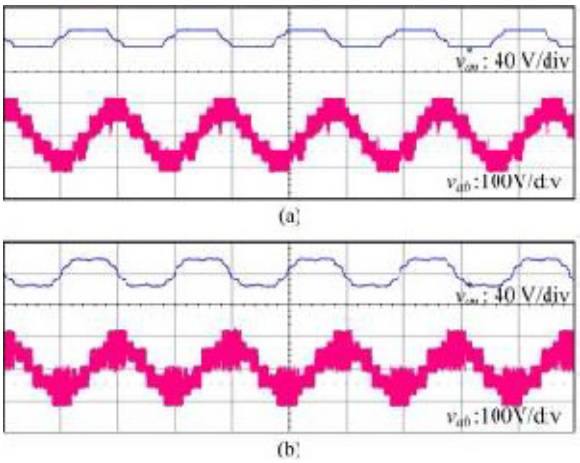

Fig. 15. Phase-a voltage reference and the line-to-line voltage between phases a and b (20 ms/div). (a) Traditional SVPWM. (b) Proposed NVM.

The voltage references are given by

$$v_{as}^{*} = V_{ph\_max} \sin(100\pi t)$$
$$v_{bs}^{*} = V_{ph\_max} \sin(100\pi t - 2\pi/3)$$
$$v_{cs}^{*} = V_{ph\_max} \sin(100\pi t + 2\pi/3). \quad (34)$$

Equation (34) is applied to the modulators of the inverter in open loop. Fig. 11 compares the voltage vector spaces and the voltage trajectories in the $\alpha-\beta$-axes of traditional SPWM, traditional SVPWM, and the proposed NVM method under the given simulation condition. Compared to the balanced dc-link case, the area of the voltage vector space is reduced under the unbalanced dc-link condition. In the figure, the traditional SPWM shows the worst voltage distortion and the minimum voltage vector space. The traditional SVPWM gives more area than SPWM, but still, the voltage distortion is not avoidable.

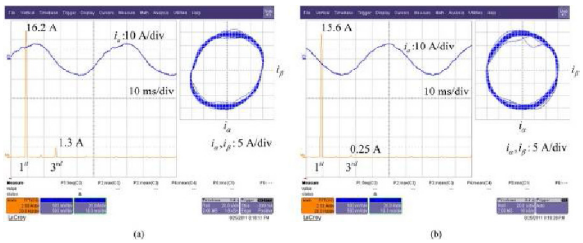

Fig. 16. Comparison of the FFT results and the current trajectories in the $\alpha-\beta$ plane. (a) Traditional carrier-based SVPWM. (b) Proposed NVM.

The proposed method shows no distortion on the output voltage and maximizes the voltage vector space compared to other methods. Fig. 12 shows the time-domain simulation results with the same simulation condition. From $t = 0.0$ s to $t = 0.05$ s, traditional SPWM is used. From $t = 0.05$ s to $t = 0.1$ s, traditional SVPWM is used. After $t = 0.1$ s, the proposed method is applied. When traditional SPWM is applied, *vsn* is zero, and the pole voltage references are identical to the ones in (34). With traditional SVPWM, *vsn* is no longer zero, and the peak voltage of the pole voltage references is reduced compared to SPWM. However, the duty reference of phase *a*, where the dc-link voltage is minimum among the three phases, is saturated in both cases. Whereas with the proposed method, the fundamental frequency component of the neutral voltage is included in *vsn*, and the duty references are not saturated. The benefit of the proposed method can also be observed from the peak value of the phase current in the last section of the figure. Under traditional methods, the phase currents are unbalanced. However, the phase currents are well balanced with the proposed method. From the simulation results, it can be seen that the proposed method can synthesize the maximum available phase voltage in the linear modulation range under unbalanced dc link.

5. Experiments

Experiments have been carried out to verify the performance of the proposed NVM strategy. Fig. 13 shows the experimental setup consisting of the developed two-by-three configuration MLCI, the power supplies, the

interior permanent magnet (IPM) motor, and the braking load. In order to drive the motor, the typical field orientation control in the synchronous reference frame is implemented with a lookup-table-based maximum-torque-per-ampere strategy. The MLCI was built by using power MOSFETs, and the proposed modulation strategy was implemented in an in-house designed 32-b digital signal processor (DSP) board, where a four-channel digital-to-analog converter is embedded to monitor the variables inside the DSP. The switching frequency for each module was chosen to be 5 kHz.

Fig. 14 compares the performances of the traditional carrierbased SVPWM and the proposed NVM strategies under Vdc_a = 16 V, Vdc_b = 48 V, and Vdc_c = 48 V. Before applying the proposed method, the shape of *vsn* is similar to a typical injected voltage in traditional carrier-based SVPWM except for a little asymmetrical component caused by the unbalanced dc links, and phase-*a* duty reference *da*1 is saturated because Vdc_a is lower than those of the other phases. In this case, the phase currents are also unbalanced, as shown in the bottom section in the figure. However, if the proposed NVM is applied, the shape of *vsn* is different from the traditional one because it includes he neutral voltage component. As a result, *da*1 is no longer saturated, and the phase current imbalance is compensated. However, phase-*b* duty reference *db*1 is greater than before. This implies that the dependent vectors in phase *a* are more utilized than before while the magnitude of the independent vectors in the phase is decreased because of the lower dc-link voltage.

Fig. 15 shows the phase voltage reference and the line-to-line voltage. The dc-link condition in this case is Vdc_a = 36 V, Vdc_b = 72 V, and Vdc_c = 72 V. As with the previous case, the phase voltage reference is saturated without the proposed method, whereas it is not saturated when the proposed method is applied.

Fig. 16 compares the fast Fourier transform (FFT) results and the trajectories of $i\alpha$ and $i\beta$ in the $\alpha-\beta$ plane with and without the proposed NVM method. Here, the dc-link condition is Vdc_a = 40 V, Vdc_b = 16 V, and Vdc_c = 48 V. In Fig. 16(a), the traditional carrier-based SVPWM is utilized, and it can be seen that *ia* is severely distorted. The fundamental and third harmonic components are evaluated to be 16.2 and 1.3 A, respectively. As can be seen in the figure, the trajectory of the phase current in the $\alpha-\beta$ plane is also distorted. The total harmonic distortion (THD) is evaluated as 7.8% in this case. On the other hand, if the proposed NVM is utilized as shown in Fig. 16(b), the phase current imbalance is compensated, and the third harmonic component is reduced by 19% of the previous condition.

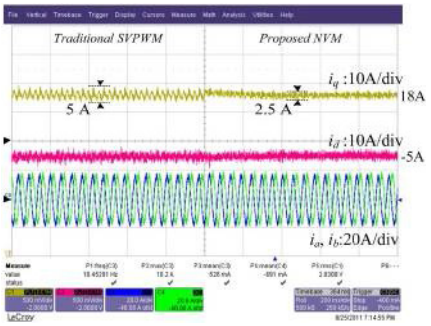

Fig. 17. *d*- and *q*-axis current responses (200 ms/div).

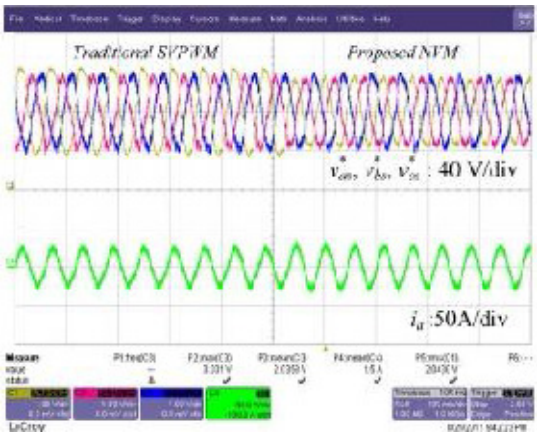

Fig. 18. Phase voltage references and *ia* (100 ms/div).

The shape of the current trajectory in the $\alpha-\beta$ plane is also improved, and the measured THD is about 4.13%. Fig. 17 compares the *d*- and *q*-axis currents *id* and *iq* of the IPM motor without and with the proposed method under the same dc-link condition with the previous test. Without the proposed method, both *id* and *iq* have ripple components because the output current is unbalanced. If the proposed NVM is applied, the phase current imbalance is compensated, and the ripple components are eliminated. The magnitude of the current ripple in *iq* is reduced by 50%.

In fact, balancing of the output voltage can be also verified from the phase voltage references, as shown in Fig. 18. Before applying the proposed method, the phase voltage references are highly unbalanced because of the unbalanced phase currents. However, once the proposed NVM is utilized, the phase voltage references are balanced, and the phase current becomes more sinusoidal.

In Fig. 19, the injected voltages with the traditional and proposed methods are represented as *vsn*_svm and *vsn*_nvm, respectively. Here, both the traditional and proposed methods

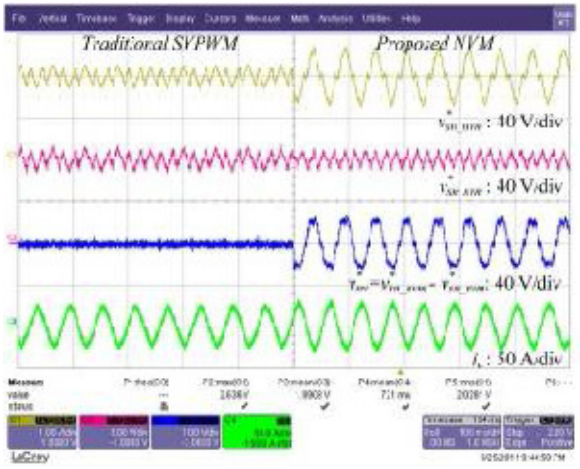

Fig. 19. Comparison of the injected voltages (100 ms/div).

In sum, these experimental results show that the proposed NVM method compensates the voltage and current imbalances under unbalanced dc-link conditions in the MLCI as well as maximizes the linear modulation range.

6. Conclusion

The NVM technique for MLCIs under unbalanced dc-link conditions has been proposed in this paper. In order to analyze the maximum synthesizable voltage of MLCIs, the voltage vector space has been analyzed using the switching function. From the analysis, the maximum linear modulation range was derived. The proposed NVM technique is applied to achieve the maximum modulation index in the linear modulation range under an unbalanced dc-link condition as well as to balance the output phase voltages. Compared to the previous methods, the proposed technique is easily implemented and improves the output voltage quality under unbalanced dc-link conditions. Both simulations and experimental results based on the IPM motor drive application verify the effectiveness of the proposed method.

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