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A Modified 8-Transistor SRAM Cell Design with High Stability and Low Power Applications

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Abstract - SRAM occupies two-third area of VLSI chips, therefore it dominates the total power consumption. To enhance the performance of these chips, SRAM cell should meet the requirement of lesser power consumption. This paper presents a new 8T SRAM cell that is efficient in Dynamic power consumption in Write mode and Leakage power consumption when compared with referred 9T SRAM cell and standard 6T SRAM cell. The design is simulated in 45-nm CMOS technology that results 18.6% reduction in Dynamic power consumption during Write mode and 28.4 % reduction in Leakage power consumption as compared to referred 9T SRAM cell. When compared with standard 6T SRAM cell this new 8T SRAM cell results 20.1 % reduction in Dynamic power consumption during Write mode and 18.1 % reduction in Leakage power consumption**.**

Keywords **- Static Random Access Memory (SRAM), Static Noise Margin (SNM), CMOS.**

1. Introduction

As the technology scales down, the feature size of CMOS devices has been proportionally reduced to smaller dimensions and results in continuous performance improvements in VLSI chips. Due to this, the variation in process parameters become a major challenging issue while designing a CMOS circuit [1-3] .SRAM cell is one of the CMOS based circuit which can be used as a basic storing element in memories that are used in personal computers, workstations, routers and peripheral equipment, internal CPU caches as well as external burst mode SRAM caches, hard disk buffers, router buffers etc. SRAM cell uses bi-stable latching circuitry made of cross coupled CMOS inverters to store each bit and it works without refreshing. While designing SRAM cell at scaled down CMOS technology, the stability and reliability of the SRAM cell may also get affected and becomes a major concern.

Stability measured in terms of Static Noise Margin(SNM) is defined as the maximum value of DC voltage tolerated by the SRAM cell without changing the stored data [4].Write SNM and Read SNM are the two parameters that defines the stability of cell in write and read mode respectively. Reliability means the ability of cell to perform the required function under stated conditions like ultra-low voltage operation etc. To have more stable and much reliable SRAM cell, many different configuration and well optimized cells are proposed in literature but the design of efficient SRAM cell is still a challenging issue. In this paper, a new 8T SRAM cell is proposed that is efficient in terms of power consumption in Write mode and Leakage power consumption in Hold mode when compared with the characteristics of referred 9T SRAM cell [5] and standard 6T SRAM cell [6].

This paper is organized as follows: - Section 2 presents the conventional SRAM cells and progressive improvements on it. Section 3 explains the Proposed 8T SRAM cell and its operation .The simulation and results of proposed 8T cell are analyzed in section 4 and final conclusion is done in section 5.

2. Conventional SRAM Cells

6T SRAM cell and 4T SRAM cell are the conventional SRAM cells which are shown in fig. 1 and fig. 2 respectively [6-7]. After summarizing the characteristics of both cells, it is found that 6T SRAM cell has better stability and data retention properties over 4T SRAM cell [8]. Due to these advantages, 6T SRAM cell is considered as the standard SRAM cell in the field of research work. But this 6T SRAM cell was also not up to the mark at nano-scaled technology because in this conventional 6T SRAM cell, the stored data is disturbed due to the voltage

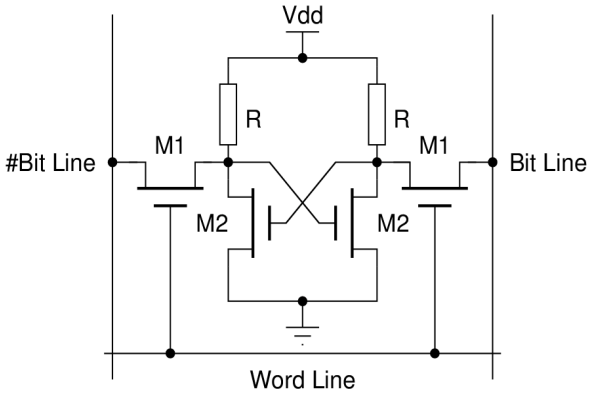

Fig. 1 4T SRAM Cell

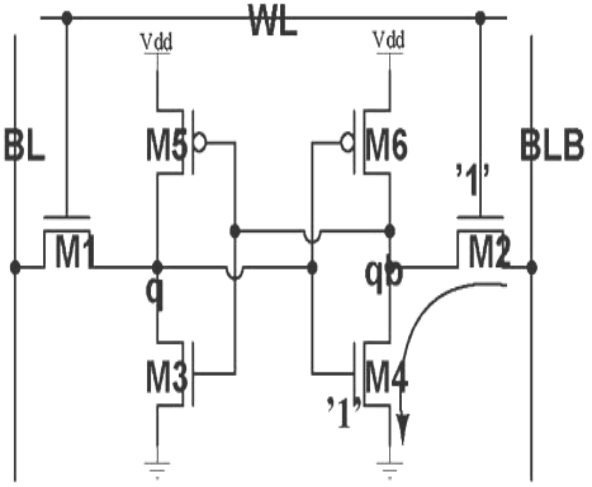

Fig. 2 6T SRAM Cell

division between the cross-coupled inverters and the access transistors during a read operation. The data is most vulnerable to external noise during this intrinsic disturbance produced by the direct-data-read-access mechanism of a standard 6T SRAM cell. So it was found that Read SNM of 6T SRAM cell was very much less as compared with Write SNM [4]. This requirement diverts most of the research work in favor of enhancing Read SNM of 6T standard cell that resulted in configuration of new SRAM cell that consumes less power along with lesser delay time.

The earlier proposed SRAM cells [9-11] were much efficient in Read SNM but the Write SNM was quite similar with standard 6T SRAM cell. In these SRAM cells, additional circuitry was added to separate the read path from storing nodes. By doing this, Read SNM becomes equal to Hold SNM. The other alternative SRAM cell [12] was designed that has improved Read SNM but at the cost of write speed performance. In the referred SRAM cell (9T SRAM), the read path was isolated from storing nodes as done in previously discussed cells. In addition, the leakage current of 9T SRAM cell was reduced to much smaller value during read operation [5]. Cell view of this novel 9T SRAM cell is shown in fig. 3. Moreover in this novel 9T SRAM cell, single ended read operation reduces the switching power of the single ended bit line and the W/L ratio of 9T cell is optimized to have appropriate values of stability, performance and soft error tolerance for better performance of the cell. The write operation of novel 9T SRAM cell was similar to standard 6T SRAM cell having same power consumption during write mode as well as leakage power consumption during hold mode. So here is the scope to enhance the performance of novel 9T SRAM cell during write and hold mode by reducing its power consumption.

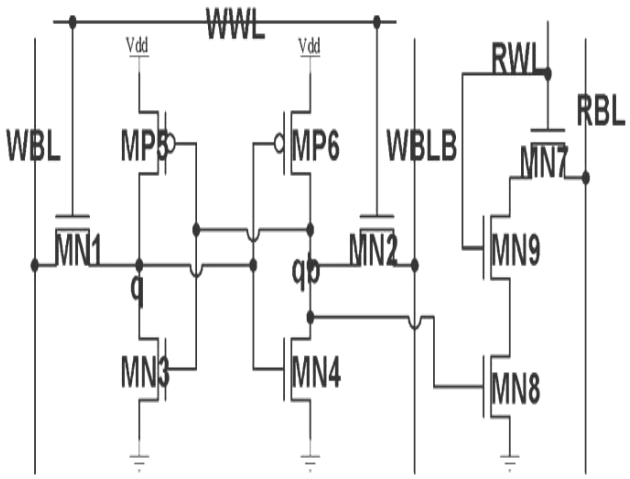

Fig. 3 9T SRAM Cell

3. Proposed 8T SRAM Cell

The overview of proposed 8T SRAM cell and the corresponding W/L ratio for MOS transistors is shown in the fig. 4. On comparing with the referred 9-T SRAM cell, this new cell has smaller modification at configure level that enhance its performance during write and hold mode. The W/L ratio for various transistors in proposed 8T SRAM cell along with the read operation and read path is same as that in referred 9T SRAM cell. In the proposed 8T SRAM cell, a single transistor (MN1) replaces the transistors MN1 and MN2 of 9T SRAM cell. In this new 8T SRAM cell, the cross coupled inverters formed by MP5, MP6, MN3 and MN4 transistors are directly connected to WBL and WBLB bit-lines. The transistor MN1 couples the two cross-coupled inverters. The transistor MN7, MN8 and MN9, connected similarly as in referred 9T cell, forms an efficient read path and

thus separating the read path from storing nodes. By setting the same W/L ratio in this 8T SRAM cell as in 9T SRAM cell, the 8T cell becomes efficient in stability, performance and soft error tolerance.

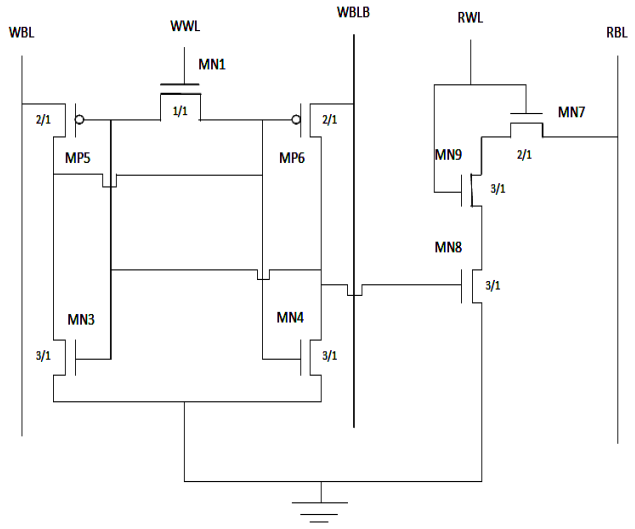

Fig. 4 Proposed 8T SRAM Cell

During the Hold mode, RWL signal is asserted low to make read path in-active. The WWL signal is asserted low which causes the M5 transistor to be in off state and thus the two inverters are not coupled through M5 transistor. The bit-lines in the 8T SRAM cell are always charged to VDD which provide the supply voltage to the cell. The data is retained by the cross coupled inverters. During Read mode, data is sensed by a sense amplifier through RBL bit-line which is pre-charged to VDD at the start of clock cycle. When the RWL signal is asserted high, the transistors MN7, MN8 and MN9 make a path for RBL bit-line to discharge or not to discharge depending upon the contents of the cell at storing nodes. Finally data is read from the bit-line by the sense amplifier.

During Write mode, data bit is written into the cell through WBL and WBLB bit lines. To write '1' bit into the cell, WWL is asserted high. The bit-line WBL remains charged to VDD and the bit-line WBLB is discharged to 2/3 VDD. Due to this, WBLB bit-line reduces the current flow into the cell which causes the output of inverter connected to this bit-line to become zero and the bit '1' is stored. Similarly to write '0', WWL is asserted high. The bit-line WBLB remains charged to VDD and bit-line WBL is discharged to 2/3 VDD which causes the WBL bit-line to reduce the current flow into the cell and thus the output of inverter connected to this bit-line becomes zero. Finally the '0' bit is stored into the cell. The waveform view of Hold mode, Write mode and Read mode is shown in fig. 5.

4. Simulation and Results

The proposed 8T SRAM cell has been successfully designed and simulated in Tanner Tools using 45nm technology file with a supply voltage of 0.8 V. The Dynamic power consumption in write mode and Leakage power consumption of the proposed 8T SRAM cell is computed for data bits. The write mode Dynamic power consumption and Leakage power consumption of proposed 8T SRAM cell is compared with referred 9T SRAM cell and standard 6T SRAM cell. The comparison results are shown in the table. 1.

Table 1: Comparison of various SRAM Cells

SRAM cell	Write mode power consumption (µW)		Leakage power consumption (pW)	
	For bit '1'	For bit '0'	For bit '1'	For bit '0'
Proposed 8T SRAM cell	13.10	13.50	1.727	1.425
Referred 9T SRAM cell	16.10	18.60	2.414	2.111
Standard 6T SRAM cell	16.40	18.60	2.111	2.111

As shown in the table, the Dynamic power consumption in write mode of proposed 8T SRAM cell is13.1µW. It is reduced by 18.6% and 20.1% when compared with referred 9T SRAM cell and standard 6T SRAM cell respectively. The Leakage power consumption of proposed 8T SRAM cell is 1.727pW and it is reduced by 28.4 % and 18.1% when compared with referred 9T SRAM cell and standard 6T SRAM cell respectively.

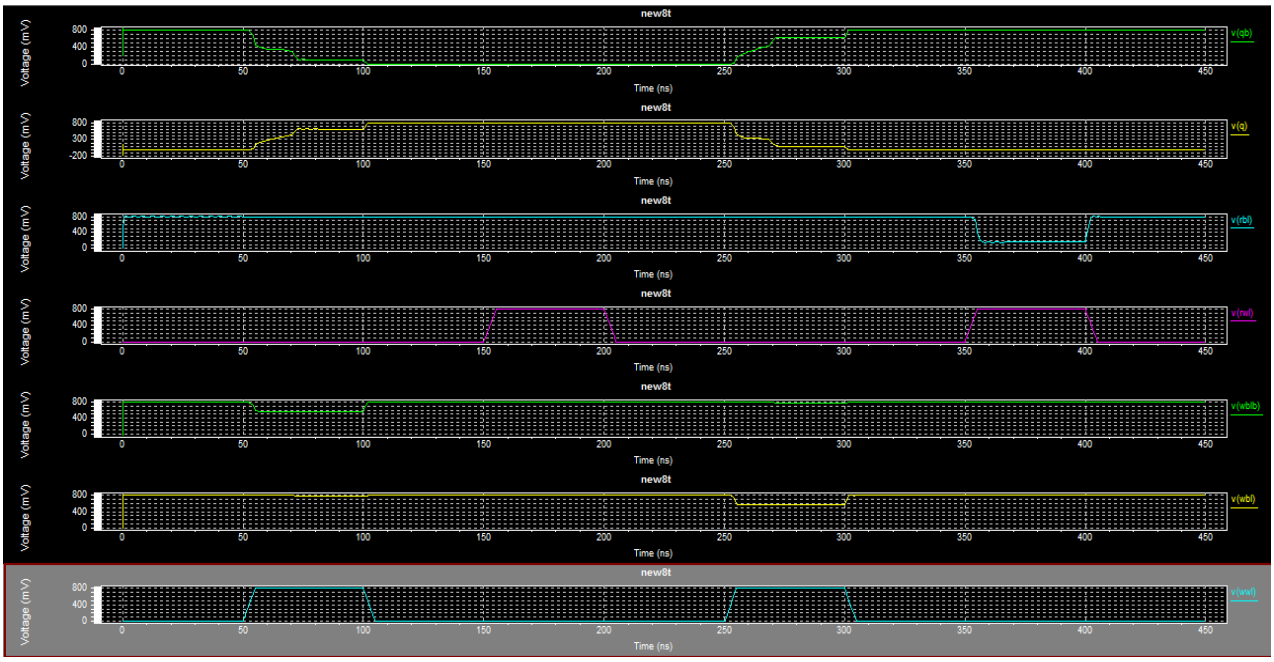

Fig. 5 W-Edit view of proposed 8T SRAM

5. Conclusion

In this paper, 8T SRAM cell is proposed in which a way of accessing the cell during the write operation is changed and also the discharging level of bit-line is increased to 2/3 VDD. Due to this, it is found that the Leakage power consumed by this proposed 8T SRAM cell is reduced by 28.4 % and 18.1% when compared to referred 9T SRAM cell and standard 6T SRAM cell respectively. The Dynamic power consumption in write mode of proposed 8T SRAM cell is also reduced by 18.6 % and 20.1% when compared with referred 9T SRAM cell and standard 6T SRAM cell respectively. Further work can be done to analyze the write speed and area consumption of proposed 8T SRAM cell.

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