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NIOS II Based Embedded Web Server Development for Networking Applications

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Abstract - This paper presents Design of NIOS II Based Embedded web server for networking applications. The ALTERA's SOPC (System on Programmable chip) Development tool is used to implement the system, which contains NIOS II Core Processor. It includes development of Embedded WEB Server application design based on the µCLINUX Kernel. The Hardware Device is based on FPGA and describe through VHDL. We have used CYCLONE II family of FPGA EP2C20C484C7 to base the prototype and NIOS II soft-core processor to run application algorithm.

Keywords **- Field Programmable Gate Array (FPGA), NIOS II, SOPC, µCLINUX, Embedded Web server.**

1. Introduction

In the past few years, embedded systems have been changing or lives are used in the diverse range of products, such as mobile phones, Home appliances, Medical equipments, Automation, Automation Robotics and so on. System on Programmable chip (SOPC) is currently the primary interest in the embedded system and digital design due to good time to market ratio. It enables designers to employ a large FPGA that contains both logic elements along with the intellectual property (IP) Processor core to implement a computer and custom hardware on a System on Chip Applications. In recent years, several commercial RISC Processor core have been introduced [1].

Embedded System architecture design is the task of selecting and programming a suitable configuration of components for a given system applications. Programmable chip companies with the help of Moore's law are providing us to be relatively straightforward use a microcontroller for flexibility and hardware peripherals are specialized functions. Now designers can add multiple component types(e.g. FPGA, DSP, and Application- specific Instruction Set Processors) to find the optimum over multiple design objectives, including system flexibility, power consumption, design cost, less maintenance and design time. A central Idea is the hardware/software co design is to merge two design processors: hardware design uses spatial decomposition and is well suited for flexibility. Among programmable components, FPGA platforms have been very successful in providing a target that equally suits software design and hardware design. Today reprogrammable Field Programmable Gate Arrays (FPGAs) are increasingly attracting the attention of developers of safety and mission critical applications for a number of reasons. First of all , modern FPGA devices offer an unprecedented level of resources (Logic memory, interconnection, arithmetic and processing resources) that make them highly competitive with ASIC in markets where low production volume and short time to market are crucial. Secondly, Reprogrammable FPGA offer a competitive advantage with respect to ASICs in being reconfigurable.

2. Literature Review

In the year 2007, Peter Yiannacouras, Proposed "Exploration and Customization of FPGA Based Soft Processors" as embedded systems designers increasingly use Field Programmable Gate Arrays (FPGA) this techniques capitalizes on these tradesoffs to improve the efficiency of softcore processors for specific applications.

In the year 2011, Ahmad Fairuz Muhd Amin, proposed "Development of Vehicle Communication System Using FPGA" The complexity requirements in hardware and software nowadays need a flexibility system for further enhancement in any design without adding new hardware. To overcome this problem, a System On Programmable Chip (SOPC) has been designed and developed using FPGA. In the year, June 2012 , Raghuwar Sharan Soni, Deepak Asati , proposed " Development of Embedded Web Server Configured on FPGA Using Soft-core Processor and Web Client on PC" in this paper the TCP/IP stack is ported on and Embedded Web server is developed on FPGA board using HTTP communication protocol.

3. Methodology

3.1 SOC Based Embedded System

A system on a chip (SOC) is an integrated circuit (IC) that integrates all components of a computer or other electronic system into a single chip

Advantages

- ❖ SOC designs usually consume less power and have a lower cost.
- ❖ Higher reliability than the multi-chip systems that they replace.
- ❖ Fewer packages in the design system, and assembly costs are reduced as well.

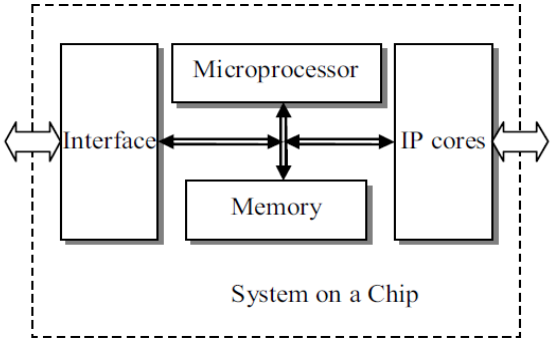

Fig.1. Basic Organization of SOC

3.2 Soft Core Processor

A soft processor is one of the Intellectual Property (IP) core that is implemented using the logic primitives of the FPGA. It is a hardware description language (HDL) model of a specific processor (CPU) that can be customized for a given application and synthesized for an ASIC or FPGA target. In many applications, NIOS II soft-core processors are several advantages over custom designed processors such as reduced cost, maintenance requirement, flexibility, platform independence and greater immunity to obsolescence.

Embedded systems are combination of hardware and software components working together to perform a specific function. Usually they contain in the embedded processors that are often in the form of soft-core processors that execute software code.

The NIOS II Soft-Core Processor is a general purpose Reduced Instruction Set Computer (RISC) processor core and the features are a Harvard memory architecture. This NIOS 2 core is widely used with ALTERA FPGAs and SOPC Builder.

The NIOS II processor is a general-purpose RISC processor core, providing features they are:

■ Processor have Full 32-bit instruction set, data path, and address space .
■ NIOS II Soft core Processor has 32 general-purpose registers.
■ 32 external interrupt sources.
■ Soft core processors Provides Dedicated instructions for computing 64-bit and 128-bit products of multiplication operations can performed.
■ Processor has Floating-point instructions for single-precision floating-point operations.

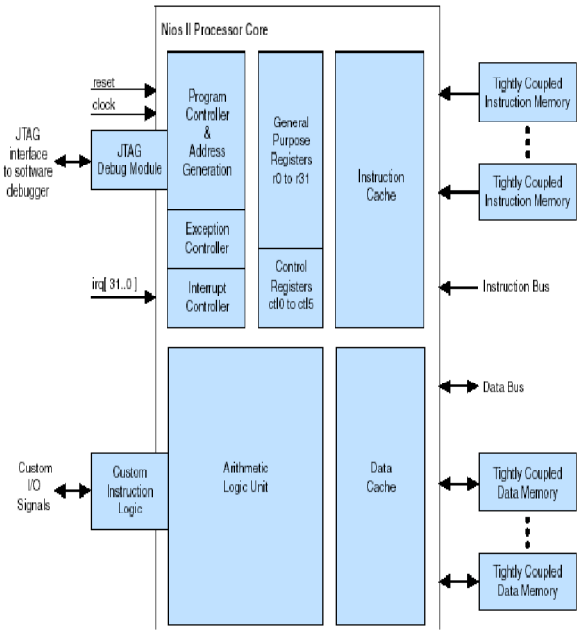

Fig.2. NIOS II Soft-core Processors

The ALTERA QUARTUS II design software provides a complete, multiplatform, multifunctional design environment that easily adapts to your specific design needs. It is a comprehensive environment for system-on-a-programmable-chip (SOPC) design in QUARTUS II . The QUARTUS II software includes solutions for all phases of FPGA and CPLD design on the de2 Board. The Quartus II software allows you to use the Quartus II Graphical user interface and command-line interface for each phase of the design flow.

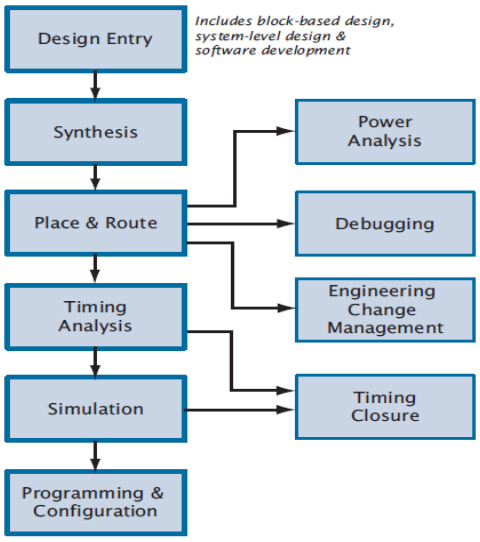

Fig.3. General NIOSII System Design Flow

3.3 ALTERA DE2 Development and Educational Board

ALTERA DE1 board become one of the most widely Development FPGA board which is used to development of FPGA design and implementations. The purpose of the ALTERA DE2 Development and Education board is to provide for learning about digital logic circuit design, computer organization, and FPGAs. ALTERA DE2 Board uses the state-of the art technology in both hardware and software of CAD tools to expose researchers and professionals to a wide range of topics. The ALTERA board offers a rich set of features that make it suitable for research work ALTERA provides a suite of supporting materials for the DE2 board. The ALTERA Board provide maximum flexibility for the user, all connections are made through the ALTERA Cyclone II FPGA device.

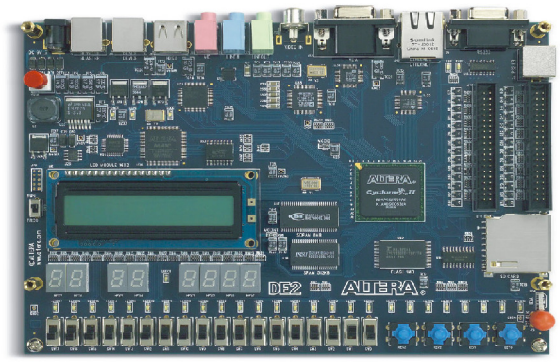

Fig.4.ALTERA DE2 Development and Educational Board

3.4 µCLINUX Kernel

µLinux is a hard real time RTOS microkernel that runs the entire Linux operating system as a fully preemptive process. It is one hard real time variant of Linux, among several, there are some applications that makes it possible to control robots, data acquisition systems, manufacturing plants, and other time-sensitive instruments and operating machines etc. RT Linux is structured as a small core component and a set of optional components.

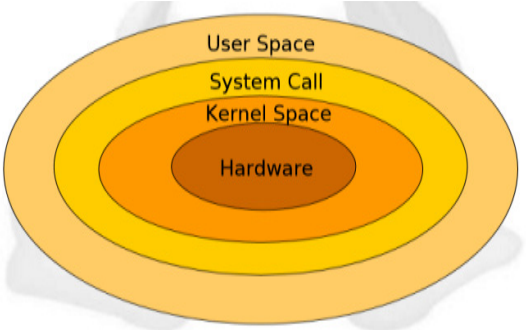

Fig.5. System Diagram of µCLINUX Kernel

4. System Architecture

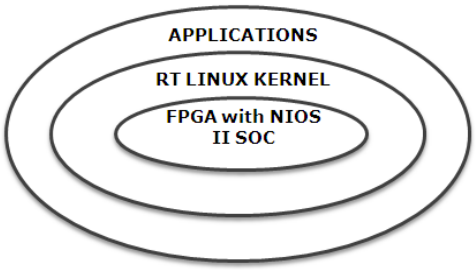

Fig.6:- System Diagram

The NIOS II processor interfaces needed to connect to other chips on the DE2 board are implemented in the Cyclone II FPGA chip. The memory blocks in the Cyclone II device can be used to provide an on-chip memory for the NIOS II processor. The implementation of embedded system with soft core based hardware implementation using programmable hardware devices like FPGA and bootable kernel loaded on that like kernel of RT Linux.

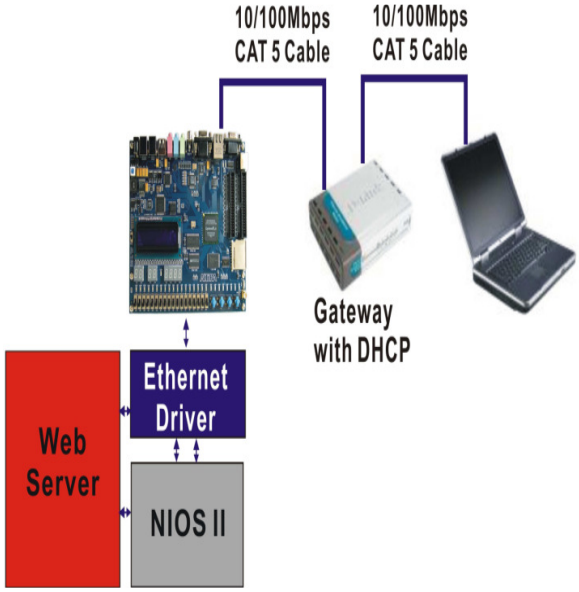

Fig.7. :-System Architecture of WEB Server Design on DE2 Board

This describes how to build a web server using DE2 board by using a NIOS II processor. The above fig.7 describes the demo setup and connections. The NIOS II processor is running LWIP (Light Weighted TCP Internet Protocol) on the MICROC LINUX /OS-II RTOS. The web server uses the industry standard sockets interface to TCP/IP Protocol. It uses DHCP protocol to requests an valid IP from the Gateway. Users can use a web browser using lan connection to examine the web page content stored in the Flash memory on the ALTERA DE2 board.

5. Proposed System

5.1 System Design Flow

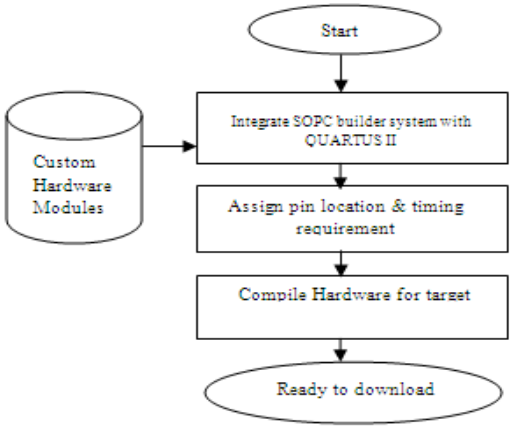

Fig.8. NIOS II System Hardware Design Flow

5.2 Flowchart

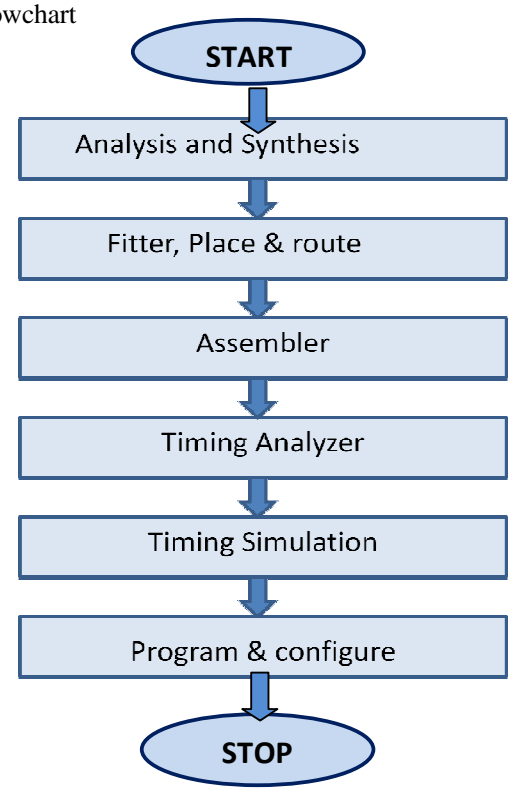

Fig.9 Flowchart of System Design

The ALTERA QUARTUS II design software provides a complete, multiplatform environment, multifunctional design environment that easily adapts to your specific system design needs. It provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design using QUARTUS II. The QUARTUS II software includes solutions for all phases of ALTERA FPGA and CPLD design. In addition, the ALTERA QUARTUS II software allows you to use the QUARTUS II Graphical user interface and command-line interface for each phase of the system design flow.

6. Advantages

It provide several advantages such as reduced maintenance cost, reduction in components, flexibility, low power consumptions in choosing specific dedicated peripheral etc. Embedded systems are hardware and software components working together to perform a specific function or dedicated task.

7. Applications

- FPGA Board can used for distributed embedded systems.
- This board can be used for providing Ethernet communication to the system in which Ethernet support is not available.

8. Result

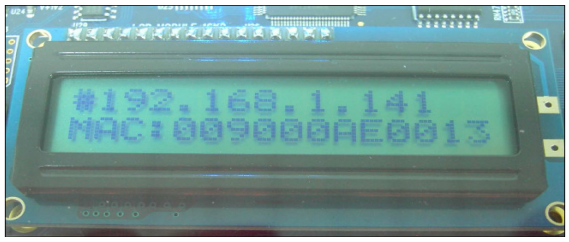

Fig 10. IP Address of Embedded webserver

9. Conclusion

This paper presented the development of WEB Server based on µCLINUX KERNEL in the NIOS II Core processors of ALTERA Cyclone II family FPGA board. The NIOS II using proved be suitable and simple to use, but requires the license. Recent development of soft-core processors on Field Programmable Gate Arrays(FPGAs) provide customization of processor to the needs of target application over traditional pre-fabricated soft core processors. NIOS II Soft-core processors are available in the form of software whose architecture and behavior are fully described by pre-designed and pre-tested Intellectual Properties (IP's), these can be synthesized on FPGAs. It provide several advantages such as reduced maintenance cost, reduction in components, flexibility in choosing specific peripheral etc.

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