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Modeling of Sigma-Delta Modulator Non-Idealities with Two Step Quantization in MATLAB/SIMULINK

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Abstract – An architecture to simplify the circuit implementation of analog-to-digital (A/D) converter in a sigma-delta (ΣΔ) modulator is proposed. The two-step quantization technique is utilized to design architecture of ΣΔ modulator. The architecture is based on dividing the A/D conversion into two time steps for achieving resolution improvement without decreasing speed. The novel architecture is designed to obtain high dynamic range of input signal, high signal-to-noise ratio and high reliability. Switched capacitor (SC) modulator performance is prone to various nonidealities, which affects overall circuit performance. In this paper a set of models are proposed which takes into account SC ΣΔ modulator nonidealities, such as sampling jitter, kT/C noise, and operational amplifier parameters (noise, finite dc gain, finite bandwidth, slew-rate and saturation voltages). Each nonidealities are modelled mathematically and their behaviour is verified using different analysis in MATLAB Simulink. Simulation results on a second-order SC ΣΔ modulator with two step quantization demonstrate the validity of the models proposed.

Keywords **- Sigma-delta (ΣΔ) modulation, signal-to-noise ratio (SNR), analog-digital conversion.**

1. Introduction

High-Resolution analog-to-digital (A/D) conversion based on ΣΔ modulation has become commonplace in many measurement applications including audio, seismic, biomedical and harsh environment sensing. ΣΔ methods incorporating oversampling and noise shaping provide improved resolution over Nyquist-rate conversion methods by trading component accuracy for time. Sigma-Delta (ΣΔ) modulators are the most suitable A/D converters for low-frequency, high-resolution applications, in view of their inherent linearity, reduced antialiasing filtering requirements and robust analog implementation.

The ΣΔ modulation relies on oversampling, which means that all the operations such as integration, A/D & D/A conversion is to be performed within the same time. If any operation takes longer time than the others, it will limit the speed and dynamic range. ΣΔ modulators can be implemented either with continuous -time or with sampled-data techniques. The most popular approach is based on a sampled-data solution with switched-capacitor (SC) implementation. In fact, SC ΣΔ modulators can be efficiently realized in standard CMOS technology and included in complete mixed-signal systems without any performance degradation. For this reason, we will focus on the case of SC ΣΔ modulators in this paper.

One bit quantization has dominated in ΣΔ modulators due to its inherent linearity. The circuit implementation also becomes very simple. The internal A/D converter can be implemented with a single comparator, and the D/A converter consists of a reference voltage, a capacitor and a couple of switches. The main drawback is the high quantization noise power generated. The signal has to be heavily oversampled in order to suppress the quantization noise.

Despite the many benefits that 1-bit quantization offers, the use of multibit quantization (Fig.2) is more useful because of the introduction of efficient dynamic element matching (DEM) techniques. The SNR can be improved by the use of multibit quantization. Most of the reported multibit ΣΔ modulators have used a moderately low number of bits in the internal quantization, although increasing the bits would have a direct impact on the overall dynamic range.

In practice, a significant problem in the design of ΣΔ modulators is the estimation of their performance, since they are mixed-signal nonlinear circuits. Due to the inherent nonlinearity of the modulator loop the optimization of the performance has to be carried out with behavioral time domain simulations. Indeed, to satisfy high-performance requirements, accurate simulations of a number of non-idealities and, eventually, the comparison of the performance of different architectures are needed in order to choose the best solution. In the design of high-resolution SC ΣΔ modulators, we have typically to optimize a large set of parameters, including the performance of the building blocks, in order to achieve the desired signal-to-noise ratio (SNR).

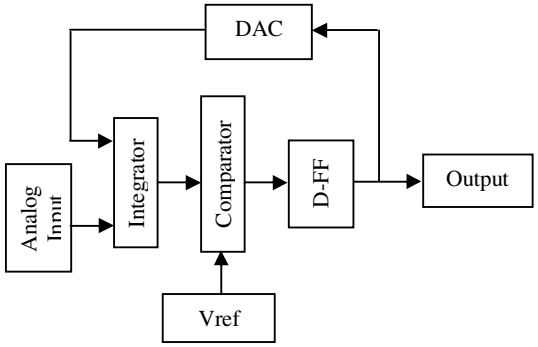


Figure 1 Block diagram of ΣΔ modulator.

Therefore, in this paper we present a complete set of SIMULINK [1] models, which allow us to perform exhaustive time-domain behavioral simulations of any ΣΔ modulator taking into account most of the non-idealities, such as sampling jitter, *kT/C* noise and operational amplifier parameters (noise, finite dc gain, finite bandwidth, slew-rate (SR) and saturation voltages).

The following sections describe in detail each of the models presented. Finally, simulation results, which demonstrate the validity of the models proposed, are provided. All the simulations were carried out on classical 2^{nd} -order SC ΣΔ modulator architecture.

2. Proposed Architecture

In multibit quantization, A/D conversion has to be performed during a single clock cycle. The conversion result has to be available to the feedback DAC well before the next integration phase, or the loop will be unstable. This leaves the flash architecture as the only option for the internal A/D converter. Here the input signal is simultaneously compared with $2^N - 1$ reference voltages in order to decide the quantization level. This means that $2^N - 1$ comparators are needed to perform the conversion (Fig. 3). Clearly, the power consumption and the area requirement of such an A/D prohibit a large number of bits. Multibit ΣΔ modulator with two step quantization process (Fig. 4) is based on dividing the A/D conversion into two steps.

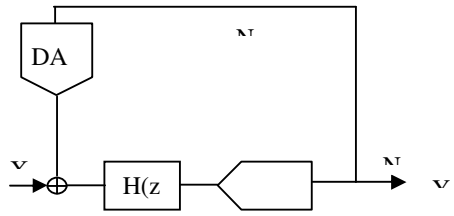


Fig. 2. A ΣΔ modulator with multibit quantization.

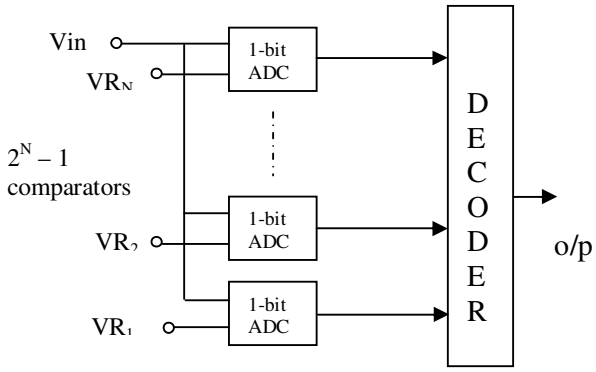


Fig. 3. Flash type converter with an input digital latch.

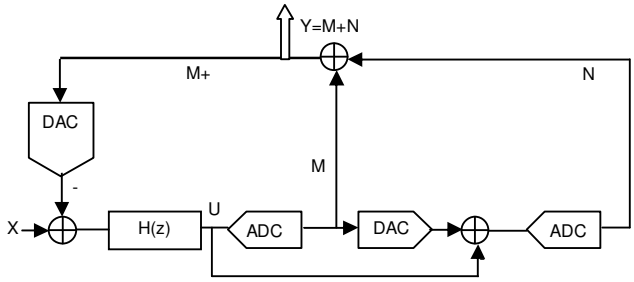


Fig. 4. A multibit ΣΔ modulator with the proposed two-step quantization.

A flash-type converter with *M*-bits resolution performs the first coarse conversion (ADC1). The output of the loop filter *U* is sampled by an MDAC at the same time the ADC1 is triggered (an MDAC implements the DAC and subtraction). Then the difference between the coarse conversion result and the sampled loop filter output *U* is amplified by the next *N*-bit flash converter ADC2. The outputs from two stages are added digitally, resulting in feedback word *M+N* bits.

3. Two-Step Internal Quantizer

To avoid some of problems encountered with a full-flash converter, the two step quantizer was developed. This two-step method uses a coarse and fine quantization to increase the SNR and resolution of the converter. The

overall accuracy of the converter is dependent on the first ADC. The second flash ADC should have only the accuracy of a stand-alone Flash converter, that means for 8-bit two-step quantizer, the second flash needs only to have the resolution of a 4-bit which is not difficult to achieve. The DAC must also be accurate to within the resolution of the ADC.

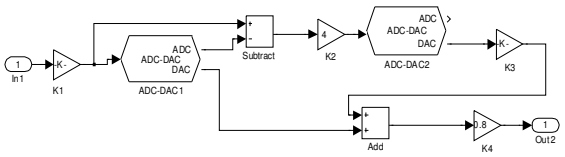


Fig. 5. A ΣΔ modulator with multibit quantization

The model of two-step quantizer is shown in Fig. 5. This model was designed and simulated in MATLAB SIMULINK.

Constants have to be correctly set for two-step quantization process.

$K_1 = 1/(2^{N/2})$, $K_2 = 2^{N/2}$), $K_3 = 1/(2^{N/2})$, $K_4 = 1/\{1+(1/2^{N/2})\}$ (1)

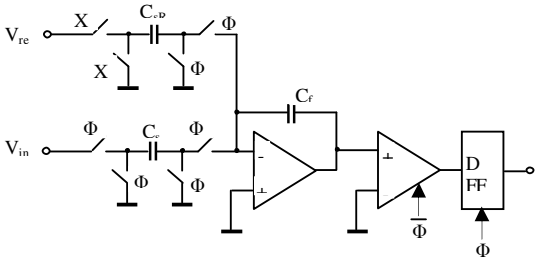


Fig. 6. Schematic of an SC first-order ΣΔ modulator.

4. ΣΔ Modulator Nonidealities

The block diagram of a first-order ΣΔ modulator is shown in Fig. 1. The modulator consists of an input sampler, an integrator, a quantizer/comparator and a feedback digital-to-analog converter (DAC). In the ΣΔ modulator, the difference between the analog input signal and the output of the DAC is the input into the integrator. The integrator integrates over each clock period. The input to the integrator is the difference between the two pulses. The integration of the pulse difference is linear over one clock period. This integral then digitized by a clocked quantizer, and the quantizer output is the output of the ΣΔ modulator. In the feedback path, the DAC shifts the logic level so that the feedback term matches the logic level of the input; making the difference equally weighted.

The schematic of a first-order SC ΣΔ modulator is shown in Fig. 6. This circuit is used to introduce the nonidealities which affect the performance of SC ΣΔ modulators of any order. The main nonidealities of this circuit which are considered in this paper are the following:

1) clock jitter;
2) switch thermal noise;
3) operational amplifier noise;
4) operational amplifier finite gain;
5) operational amplifier BW & SR;
7) operational amplifier saturation voltages.

The basic concept of the proposed simulation environment is the evaluation of the output samples in the time domain.[6]

5. Clock Jitter

The effects of clock jitter on an SC ΣΔ modulator can be calculated in a fairly simple manner, since the operation of an SC circuit depends on complete charge transfers during each of the clock phases [2].

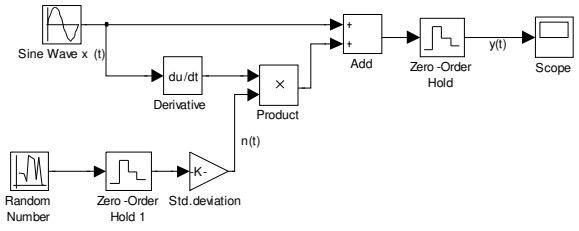


Fig. 7. Modeling random sampling jitter.

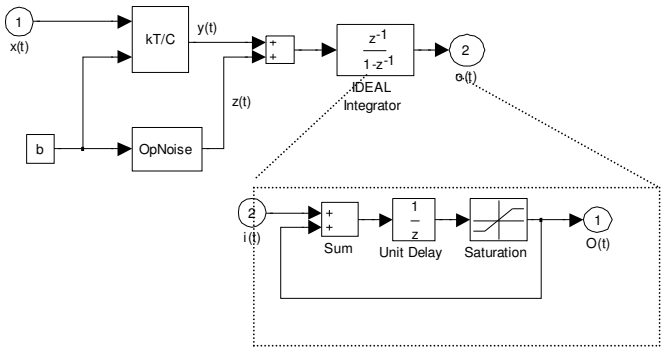


Fig. 8. Model of noisy integrator.

In fact, once the analog signal has been sampled, the SC circuit is a sampled-data system where variations of the clock period have no direct effect on the circuit

performance. Therefore, the effect of clock jitter on an SC circuit is completely described by computing its effect on the sampling of the input signal.
by

$$x(t + \delta) - x(t) \approx 2\pi f_{in}\, \delta A \cos(2\pi f_{in}\, t) = \delta \frac{d\, x(t)}{dt}. \quad (2)$$

This effect can be simulated with SIMULINK by using the model shown in Fig. 7, which implements Eqn. (2).

6. Integrator Noise

The most important noise sources affecting the operation of an SC ΣΔ modulator are the thermal noise associated to the sampling switches and the intrinsic noise of the operational amplifiers. The total noise power of the circuit is the sum of the switch noise power and the op-amp noise power. Because of the large low-frequency gain of the first integrator, the noise performance of a ΣΔ modulator is determined mainly by the switch and op-amp noise of the input stage.

These effects can be simulated with SIMULINK using the model of a "noisy" integrator shown in Fig. 4, where the variable $b = C_s / C_f$ represents the coefficient of the integrator.

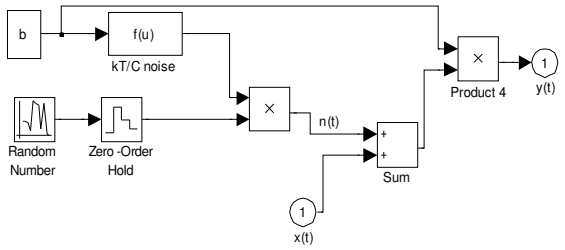


Fig. 9. Modelling switches thermal noise (kT/C block).

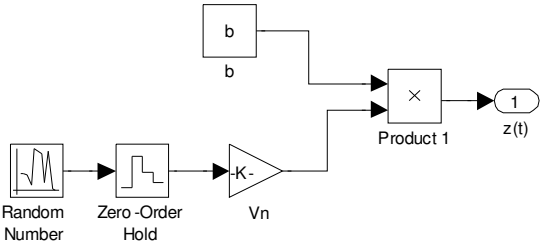


Fig. 10. Operational amplifier noise model (OpNoise block).

A. Switches Thermal Noise

Thermal noise is caused by the random fluctuation of carriers due to thermal energy and has a white spectrum and wide band, limited only by the time constant of the switched capacitors or the bandwidths of op-amps.

The error introduced when a sinusoidal signal $x(t)$ with amplitude A and frequency f_{in} is sampled at an instant which is in error by an amount δ is given

Consider the sampling capacitor Cs in the SC first order ΣΔ modulator shown in Fig. 6. This is in series with a switch, with finite resistance Ron, that periodically opens, thus sampling a noise voltage onto Cs. The total noise power can be found by evaluating the integral [3]

$$e^2_T = \int_0^\infty \frac{4kTR_{on}}{1 + (2\pi f R_{on} C_s)^2} df = \frac{kT}{C_s} \quad (3)$$

where k is the Boltzman's constant, T is the absolute temperature. The switch thermal noise voltage e_T (kT/C noise) is then superimposed to the input voltage $x(t)$ leading to

$$y(t) = [x(t) + e_T(t)]b = \left[x(t) + \sqrt{\frac{kT}{Cs}} n(t) \right] b \quad (4)$$

Eqn. (4) is implemented by the model shown in Fig. 9.

B. Operational Amplifier Noise

Fig. 10 shows the model used to simulate the effect of the op-amp noise. Here, Vn represents the total *rms* noise voltage referred to the op-amp input. The total op-amp noise power $(Vn)^2$ can be evaluated, through circuit simulation, on the circuit of Fig. 6 during phase Φ2, by adding the noise contributions of all the devices referred to the op-amp input

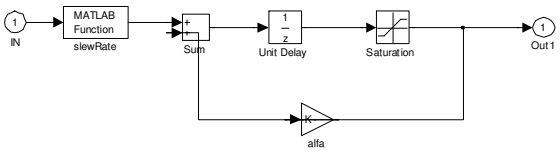


Fig. 11. Real integrator model

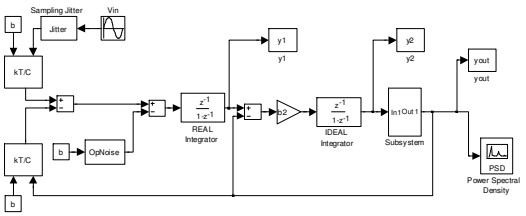


Fig. 12. Low-pass second-order ΣΔ modulator model.

and integrating the resulting value over the whole frequency spectrum.

7. Integrator Nonidealities

The SIMULINK model of an ideal integrator with unity gain is shown in the inset of Fig. 8. Its transfer function is:

$$H(z) = z^{-1} / (1- z^{-1}) \quad (5)$$

Analog circuit implementations of the integrator deviate from this ideal behavior due to several non-ideal effects. This non-ideal effect is a consequence of the op-amp non-idealities, namely finite gain and BW, slew rate (SR) and saturation voltages. Fig. 11 shows the model of the real integrator including all the non-idealities.

A. DC Gain

The dc gain of the integrator described by (5) is infinite. However, the actual gain is limited by circuit constraints. The consequence of this integrator "leakage" is that only a fraction α of the previous output of the integrator is added to each new input sample. The transfer function of the integrator with leakage becomes:

$$H(z) = z^{-1} / (1- \alpha z^{-1}) \quad (6)$$

The dc gain of the integrator H_0, therefore, becomes:

$$H_0 = H(1) = 1 / (1- \alpha) \quad (7)$$

B. Bandwidth and SR

The finite bandwidth and the SR of the op-amp are modeled in Fig. 11 with a building block placed in front of the integrator which implements a MATLAB function. [4].

TABLE I
SIMULATION PARAMETERS

Parameter	*Value*
Signal bandwidth	BW = 22.05 KHz
Sampling frequency	F_S = 11.2896 MHz
Oversampling ratio	R = 256
Samples number	N = 65536
Integrator gain	$b = b_2 = 0.5$

TABLE II
SIMULATION RESULTS

ΣΔ Modulator Parameter	*SNDR [dB]*	*Resolution [bits]*
Ideal modulator	110.5	18.06
Sampling jitter ($\Delta\tau$ = 8 ns)	102.5	16.74
Switches (kT/C) noise (Cs = 2.5 pF)	104.2	17.02
Input-referred op-amp noise (Vn = 50 μVrms)	104.1	17.01
Finite dc gain ($H_0 = 1 \cdot 10^3$)	101	16.48
Finite bandwidth (GBW = 100 MHz)	109.7	17.93
Slew-rate (SR = 18 V/μs)	100.3	16.38

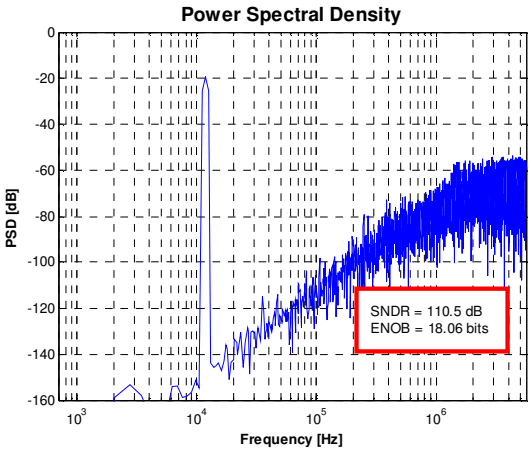
C. Saturation

The dynamic of signals in a ΣΔ modulator is a major concern. It is therefore important to take into account the saturation levels of the op-amp used. This can simply be done in SIMULINK using the saturation block inside the feedback loop of the integrator, as shown in Fig. 11.

8. Simulation Results

To validate the models proposed of the various non idealities affecting the operation of an SC ΣΔ modulator, we performed several simulations with SIMULINK on the second-order ΣΔ modulator with two-step quantization shown in Fig. 12. The simulation parameters used for the simulations are summarized in Table I and corresponds to audio standards. A minimum resolution of 18 bits is required for sensor application.

Table II compares the total SNDR and the corresponding equivalent resolution in bits of the ideal modulator, which are the maximum obtainable with the architecture and parameters used, with those achieved with the same architecture when one single limitation at a time is introduced.



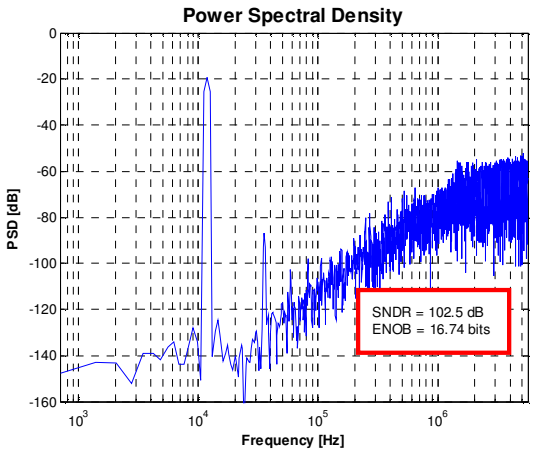


Fig. 13. PSD of (1) ideal modulator (2) with sampling jitter $\Delta\tau$ = 8 ns.

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